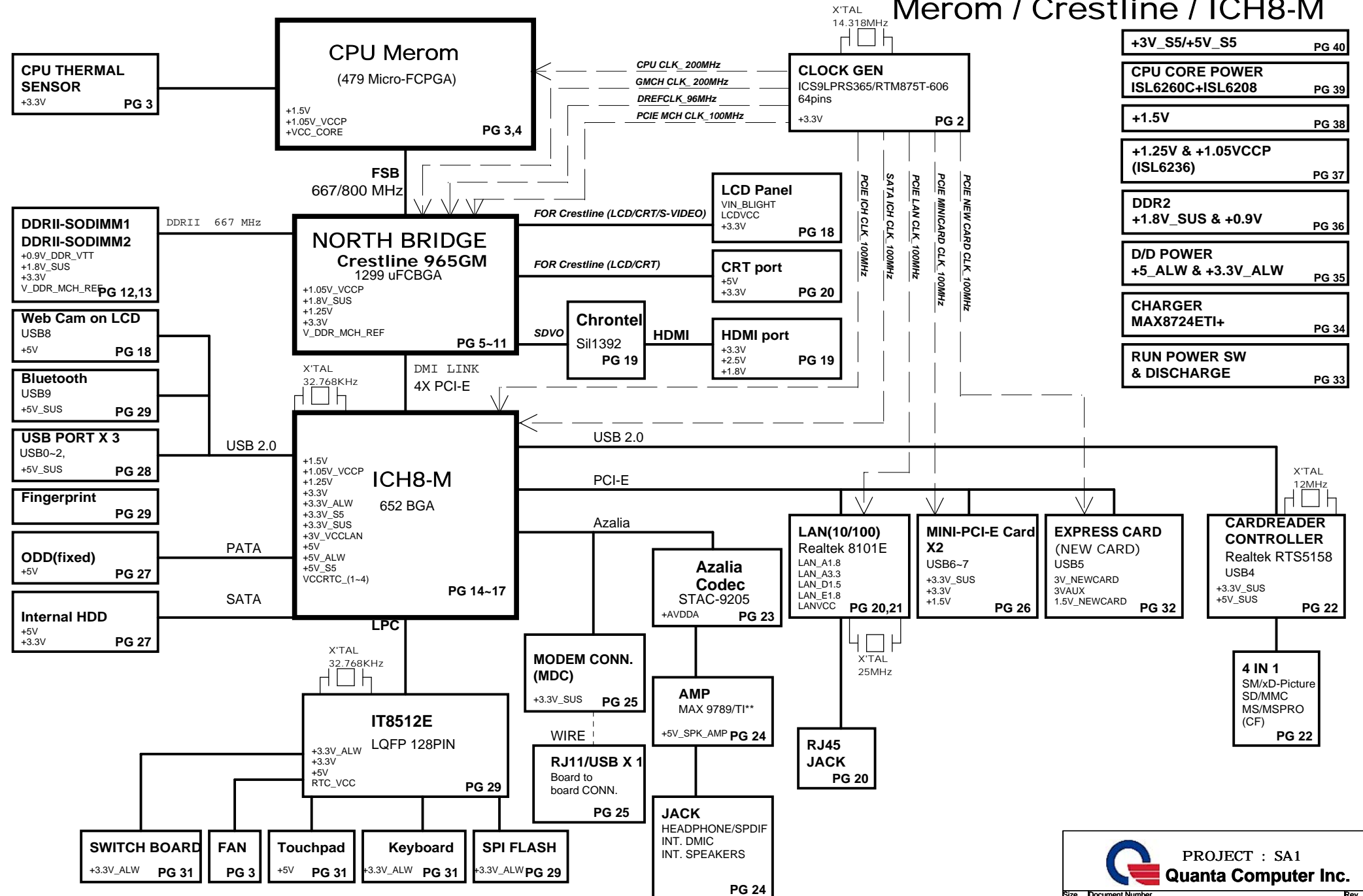
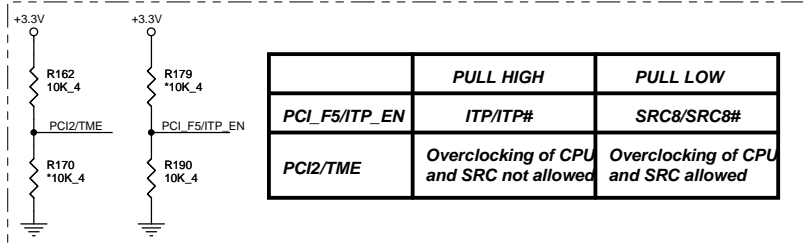
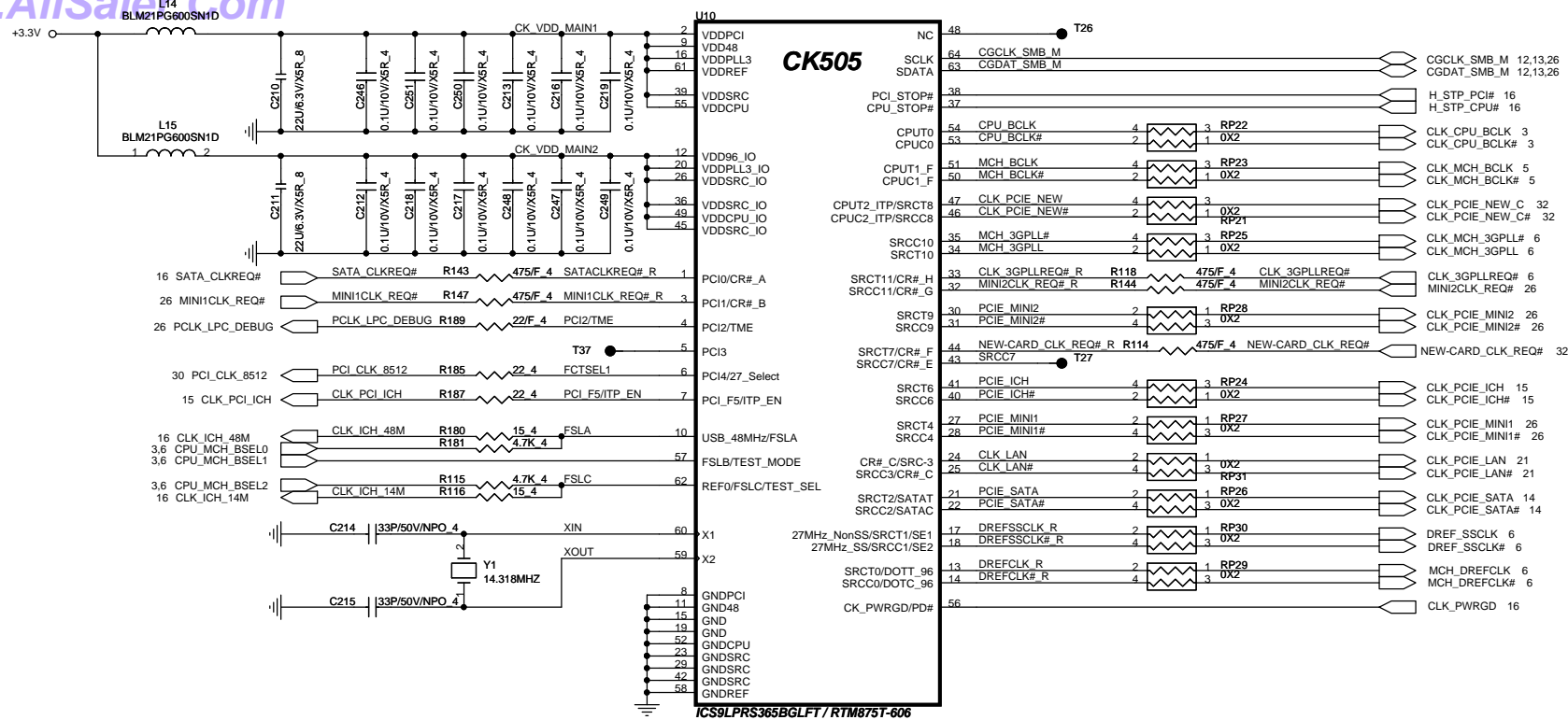


SA1 BLOCK DIAGRAM

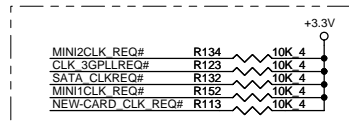
Merom / Crestline / ICH8-M



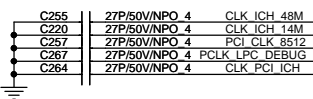


CPU Clock select

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100.00	100	33
0	0	1	133.33	100	33
0	1	1	166.66	100	33
0	0	0	200.00	100	33
0	0	0	266.66	100	33
1	0	0	333.33	100	33
1	1	0	400.00	100	33
1	1	1	200.00	100	33

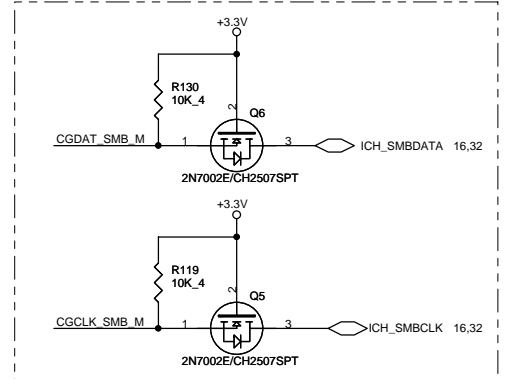
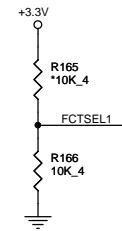


EMI CAP



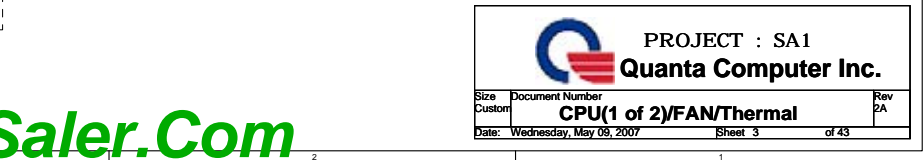
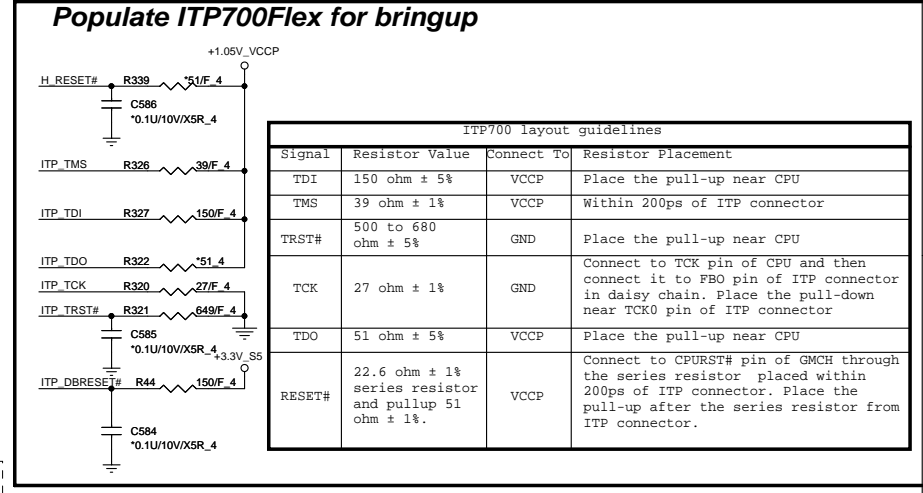
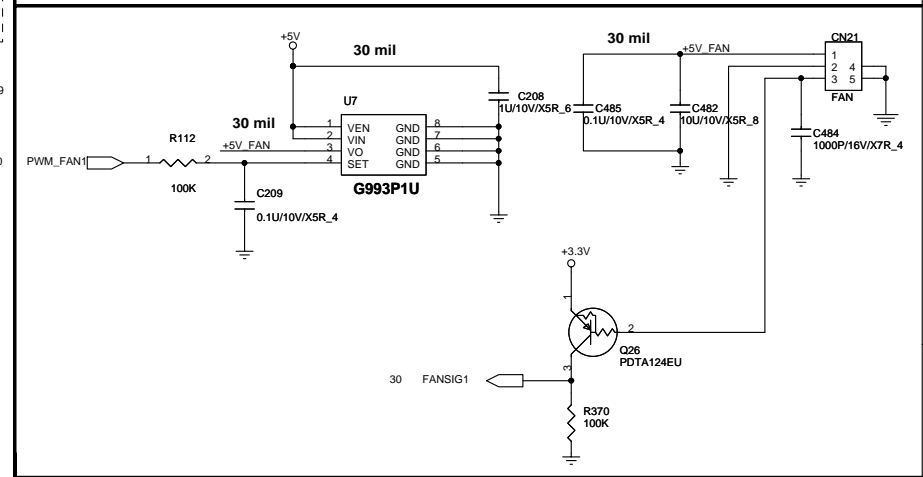
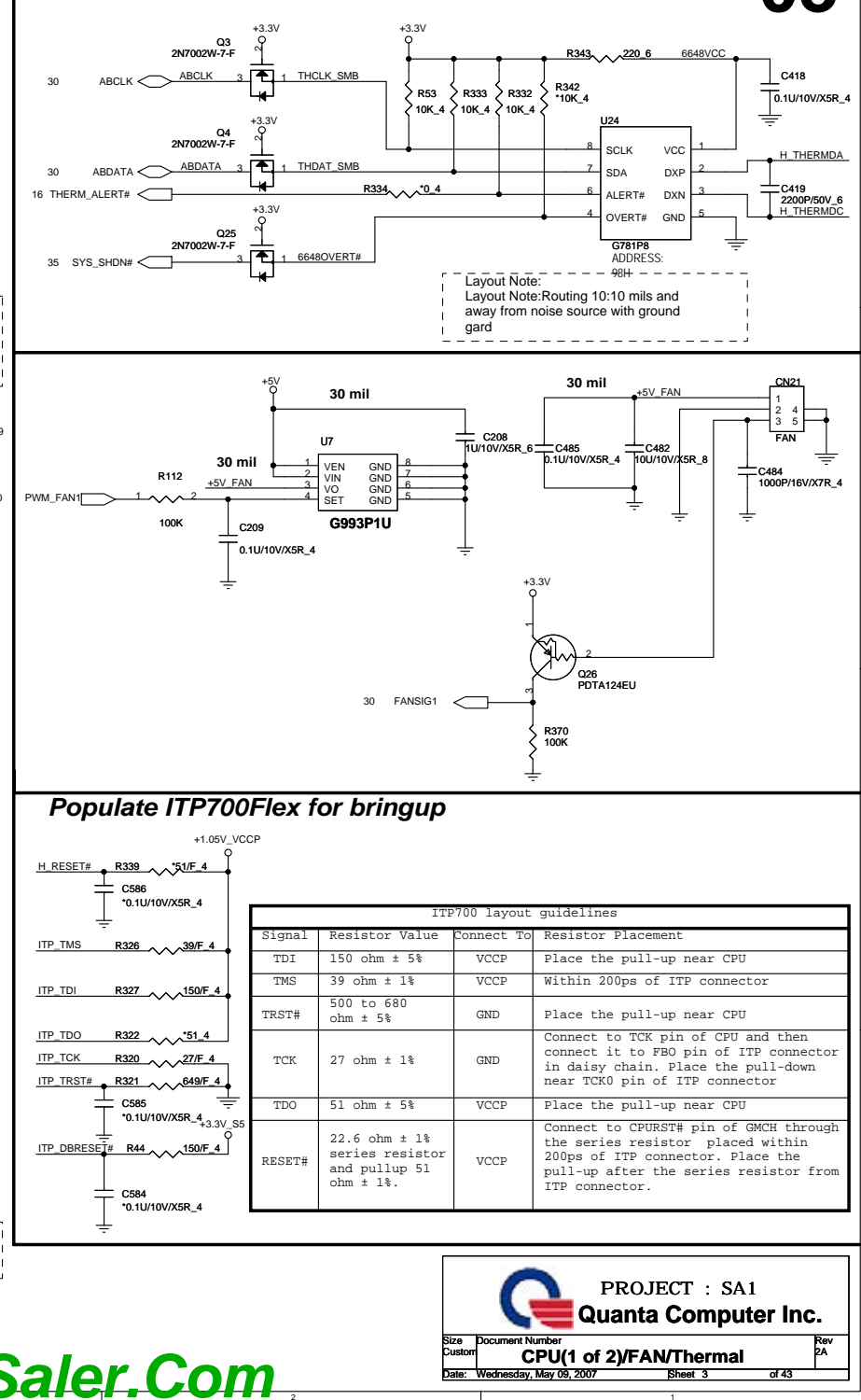
GCLK_SEL = FCTSEL1

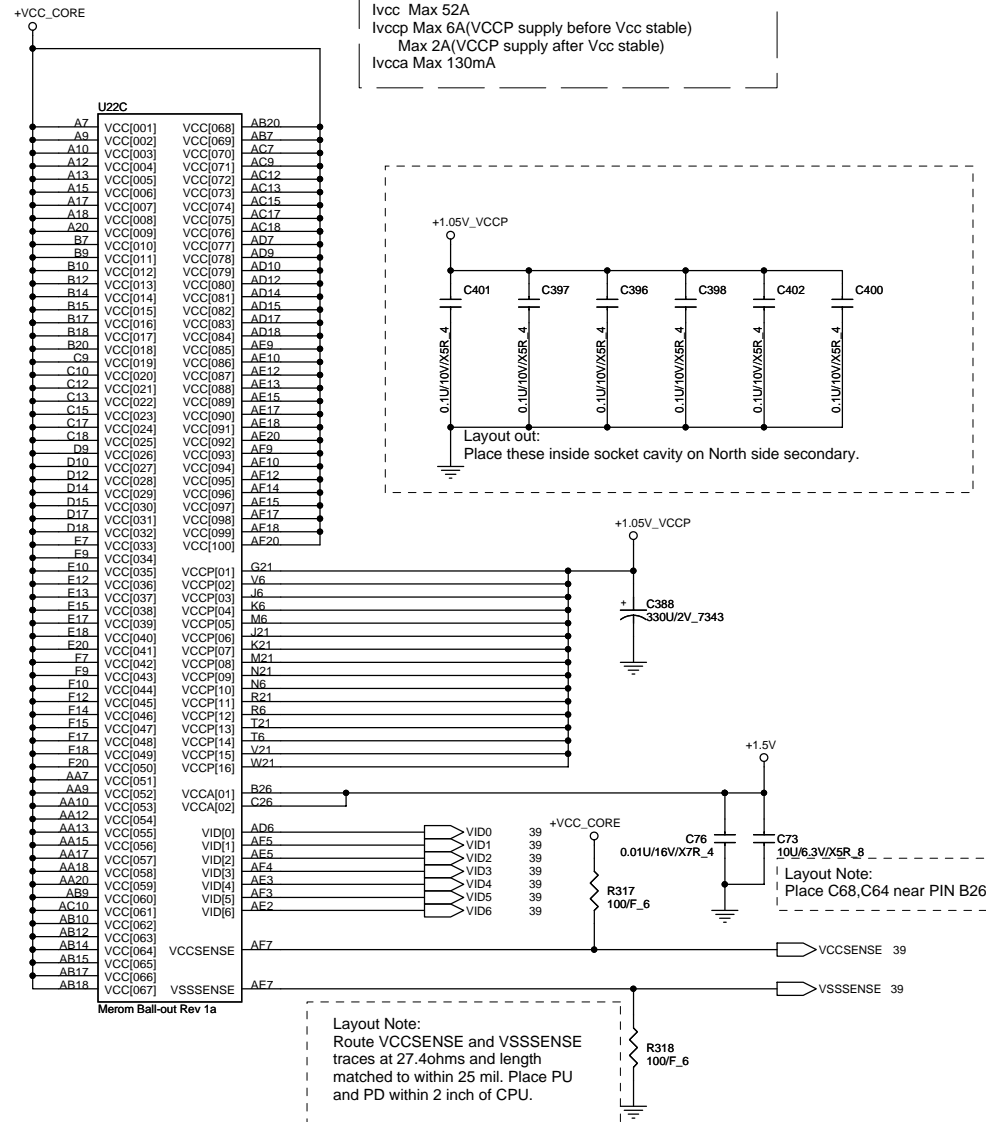
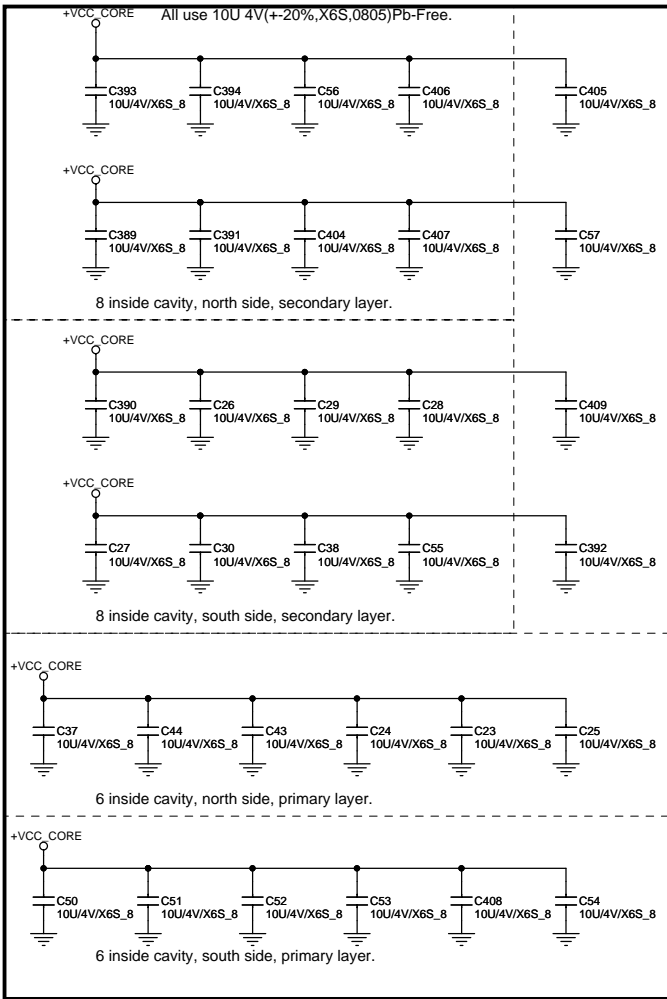
FCTSEL1 (PIN6)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96	DOT96#	SRC-1/LCDT_100	SRC-1#/LCDT_100
1 = External VGA	SRC-0	SRC-0#	27Mout-NSS	27Mout-SS



PROJECT : SA1
Quanta Computer Inc.

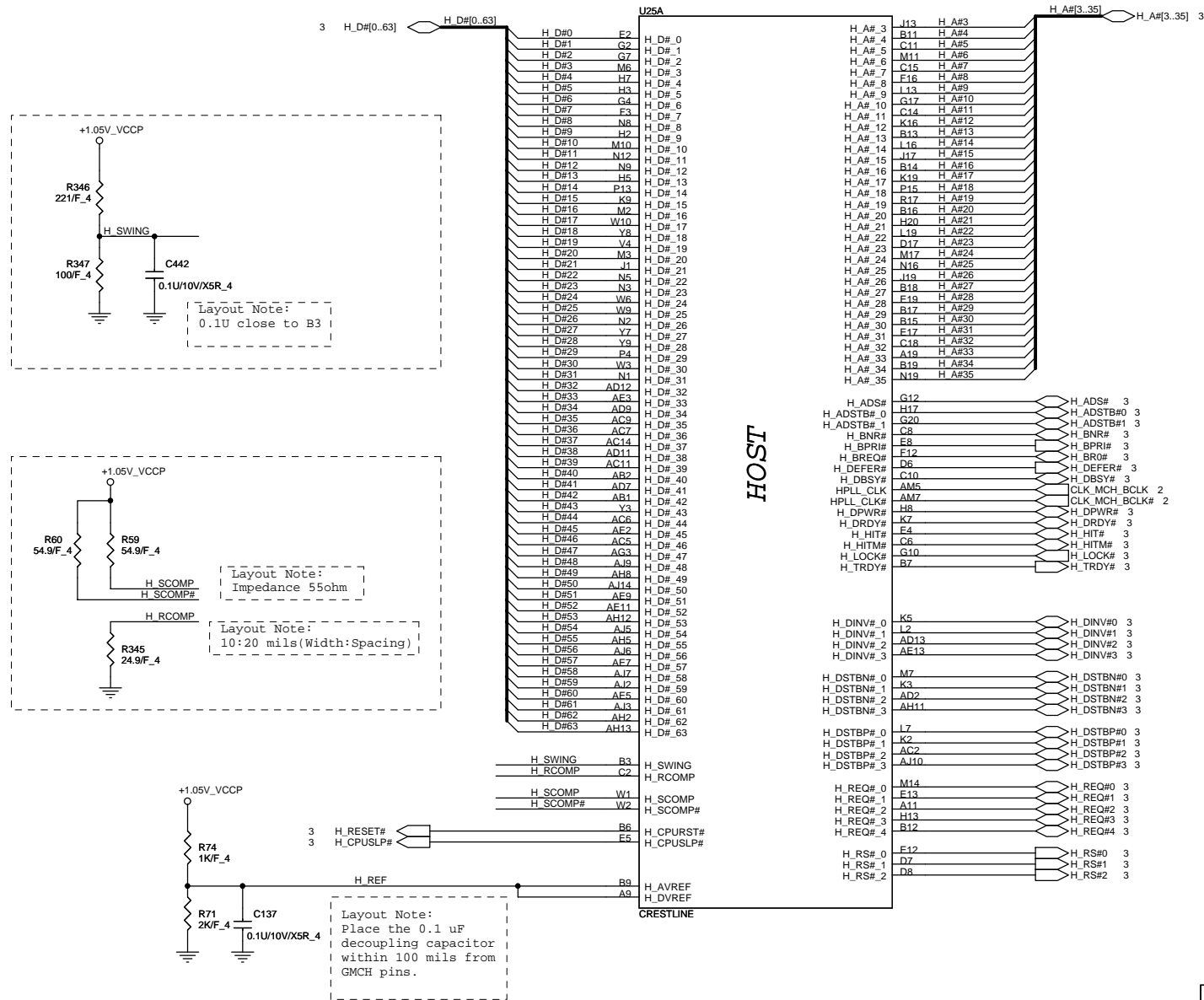
Size Custom	Document Number	Rev 2A
CLOCK GENERATOR		
Date: Wednesday, May 09, 2007	Sheet 2	of 43

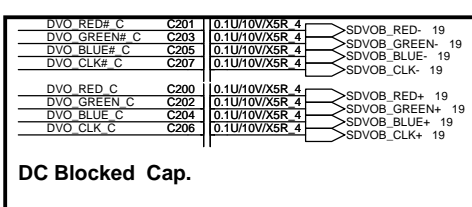


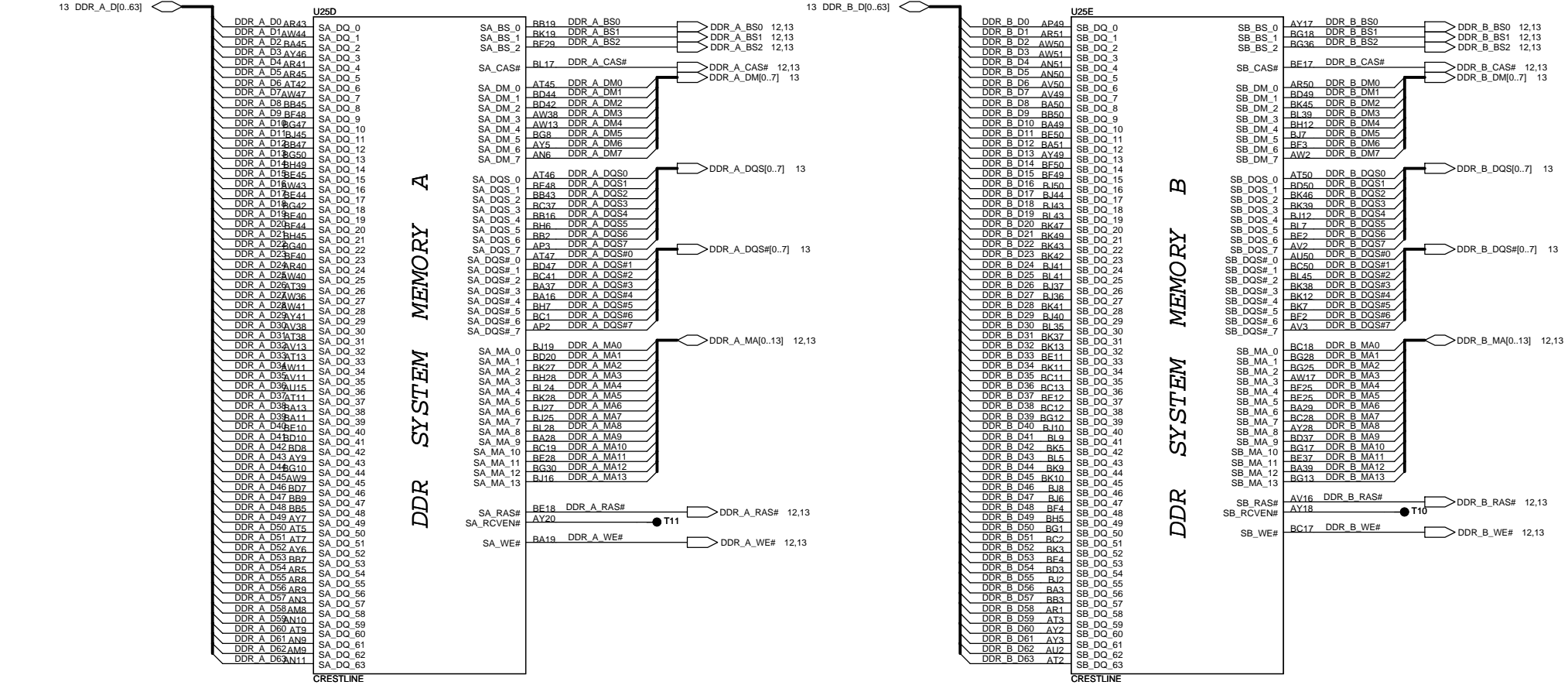


U22D

A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C3	VSS[017]	VSS[098]	V22
C8	VSS[018]	VSS[099]	V25
C11	VSS[019]	VSS[100]	W1
C14	VSS[020]	VSS[101]	W2
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C22	VSS[023]	VSS[104]	W26
C25	VSS[024]	VSS[105]	Y3
D1	VSS[025]	VSS[106]	Y6
D4	VSS[026]	VSS[107]	Y21
D8	VSS[027]	VSS[108]	Y24
D11	VSS[028]	VSS[109]	AA2
D13	VSS[029]	VSS[110]	AA22
D16	VSS[030]	VSS[111]	AA8
D19	VSS[031]	VSS[112]	AA11
D23	VSS[032]	VSS[113]	AA14
D26	VSS[033]	VSS[114]	AA16
E3	VSS[034]	VSS[115]	AA19
E6	VSS[035]	VSS[116]	AA25
E8	VSS[036]	VSS[117]	AB1
F11	VSS[037]	VSS[118]	AB4
F14	VSS[038]	VSS[119]	AB8
F16	VSS[039]	VSS[120]	AB11
F19	VSS[040]	VSS[121]	AB13
F21	VSS[041]	VSS[122]	AB16
F24	VSS[042]	VSS[123]	AB19
F26	VSS[043]	VSS[124]	AB23
G1	VSS[044]	VSS[125]	AB26
G23	VSS[045]	VSS[126]	AC3
G26	VSS[046]	VSS[127]	AC6
H3	VSS[047]	VSS[128]	AC8
H6	VSS[048]	VSS[129]	AC11
H21	VSS[049]	VSS[130]	AC14
H24	VSS[050]	VSS[131]	AC16
J2	VSS[051]	VSS[132]	AC19
J5	VSS[052]	VSS[133]	AC21
J22	VSS[053]	VSS[134]	AC24
J25	VSS[054]	VSS[135]	AD2
K1	VSS[055]	VSS[136]	AD5
K4	VSS[056]	VSS[137]	AD8
K23	VSS[057]	VSS[138]	AD11
K26	VSS[058]	VSS[139]	AD13
L3	VSS[059]	VSS[140]	AD16
L6	VSS[060]	VSS[141]	AD19
L21	VSS[061]	VSS[142]	AD22
L24	VSS[062]	VSS[143]	AD25
M2	VSS[063]	VSS[144]	AE1
M5	VSS[064]	VSS[145]	AE4
M22	VSS[065]	VSS[146]	AE8
M25	VSS[066]	VSS[147]	AE11
N1	VSS[067]	VSS[148]	AE14
N4	VSS[068]	VSS[149]	AE16
N23	VSS[069]	VSS[150]	AE19
N26	VSS[070]	VSS[151]	AE23
P3	VSS[071]	VSS[152]	AE26
	VSS[072]	VSS[153]	A2
	VSS[073]	VSS[154]	AF6
	VSS[074]	VSS[155]	AF8
	VSS[075]	VSS[156]	AF11
	VSS[076]	VSS[157]	AF13
	VSS[077]	VSS[158]	AF16
	VSS[078]	VSS[159]	AF19
	VSS[079]	VSS[160]	AF21
	VSS[080]	VSS[161]	A25
	VSS[081]	VSS[162]	AF25
	VSS[083]	VSS[163]	

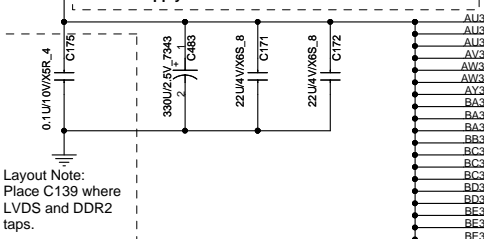






GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	12.313	

IVCCSM supply current 1 channel 1.615A 2 channel 3.138A



Layout Note:
Place C139 where
LVDS and DDR2
taps.

POWER

VCC SM

- VCC SM 1
- VCC SM 2
- VCC SM 3
- VCC SM 4
- VCC SM 5
- VCC SM 6
- VCC SM 7
- VCC SM 8
- VCC SM 9
- VCC SM 10
- VCC SM 11
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- VCC SM 34
- VCC SM 35
- VCC SM 36

VCC GFX

- VCC GFX 1
- VCC GFX 2
- VCC GFX 3
- VCC GFX 4
- VCC GFX 5
- VCC GFX 6
- VCC GFX 7
- VCC GFX 8
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- VCC GFX 31
- VCC GFX 32
- VCC GFX 33
- VCC GFX 34

CRESTLINE

VCC SM LF

- VCC SM LF1
- VCC SM LF2
- VCC SM LF3
- VCC SM LF4
- VCC SM LF5
- VCC SM LF6
- VCC SM LF7

- AW45 VCCSM LF1
- BC39 VCCSM LF2
- BE39 VCCSM LF3
- BD17 VCCSM LF4
- BD4 VCCSM LF5
- AW8 VCCSM LF6
- AT6 VCCSM LF7



VCC GFX NCTF

- VCC GFX NCTF 1
- VCC GFX NCTF 2
- VCC GFX NCTF 3
- VCC GFX NCTF 4
- VCC GFX NCTF 5
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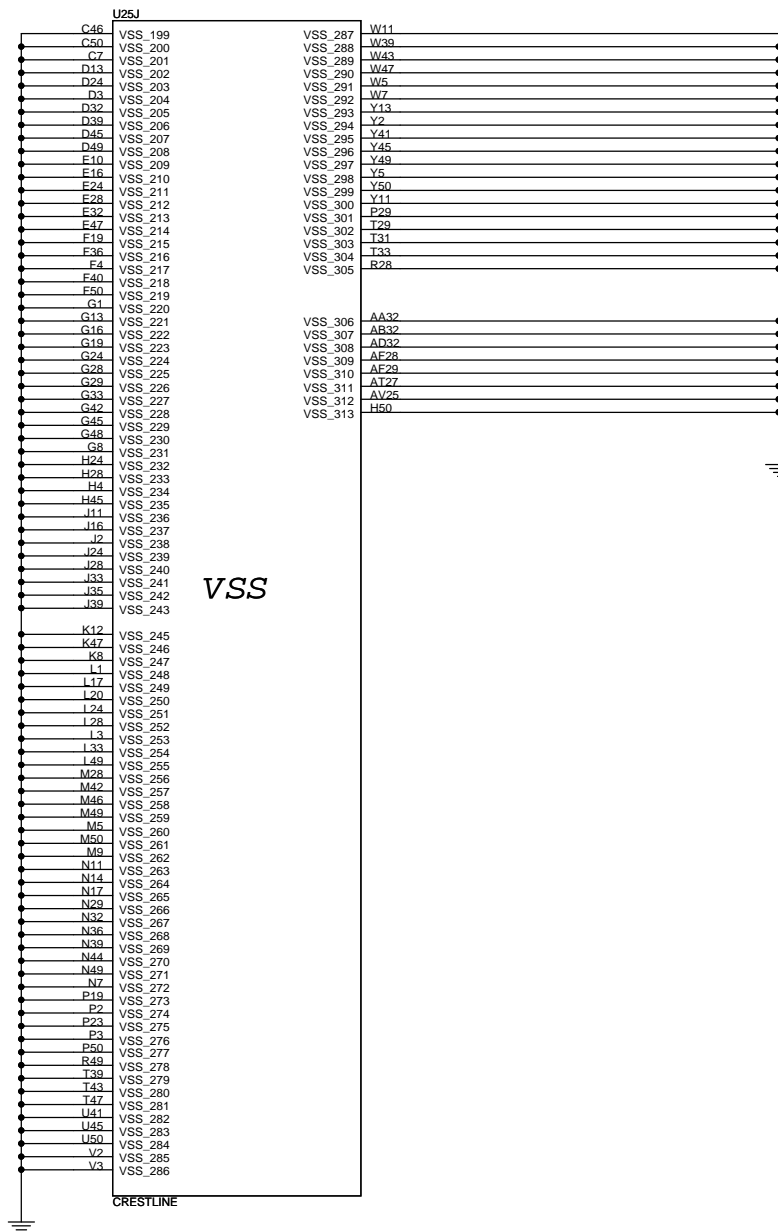
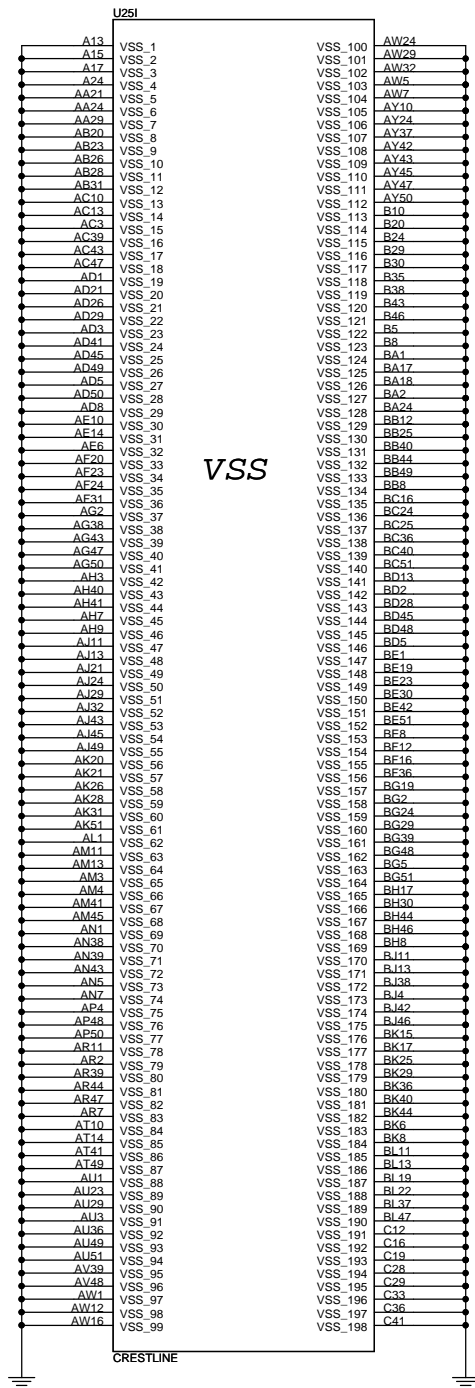
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- V99
- V100

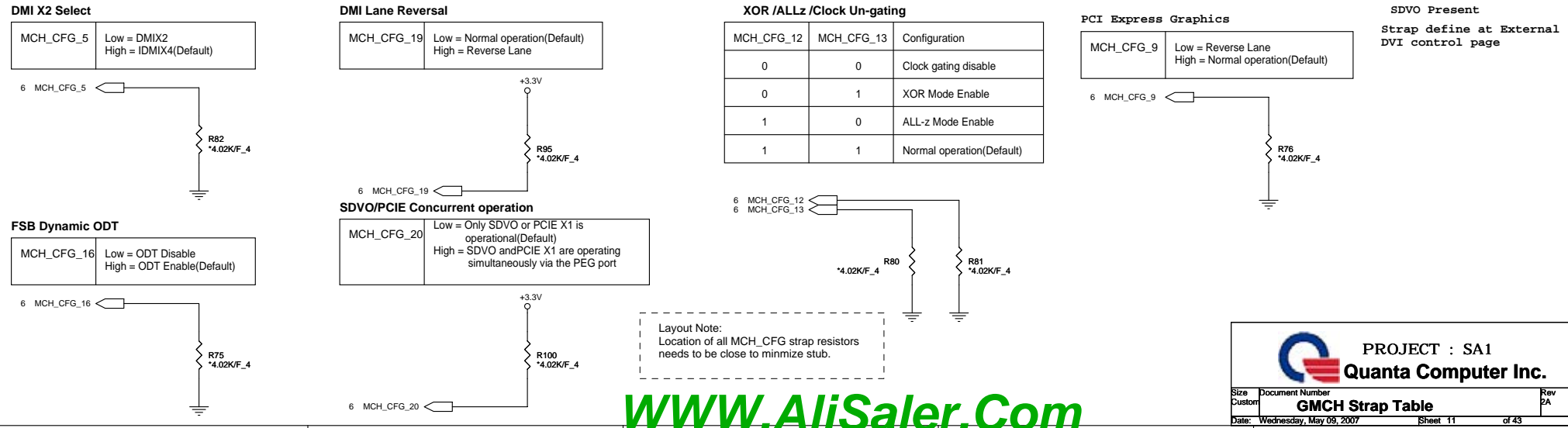
- V16
- V17
- V18</





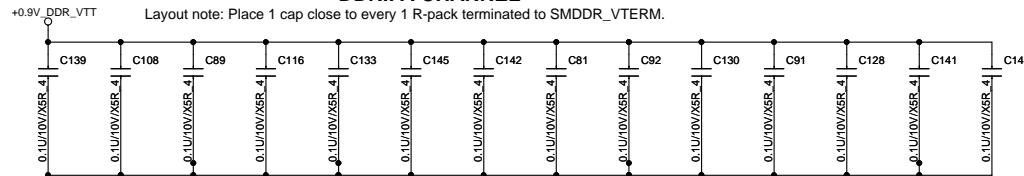
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

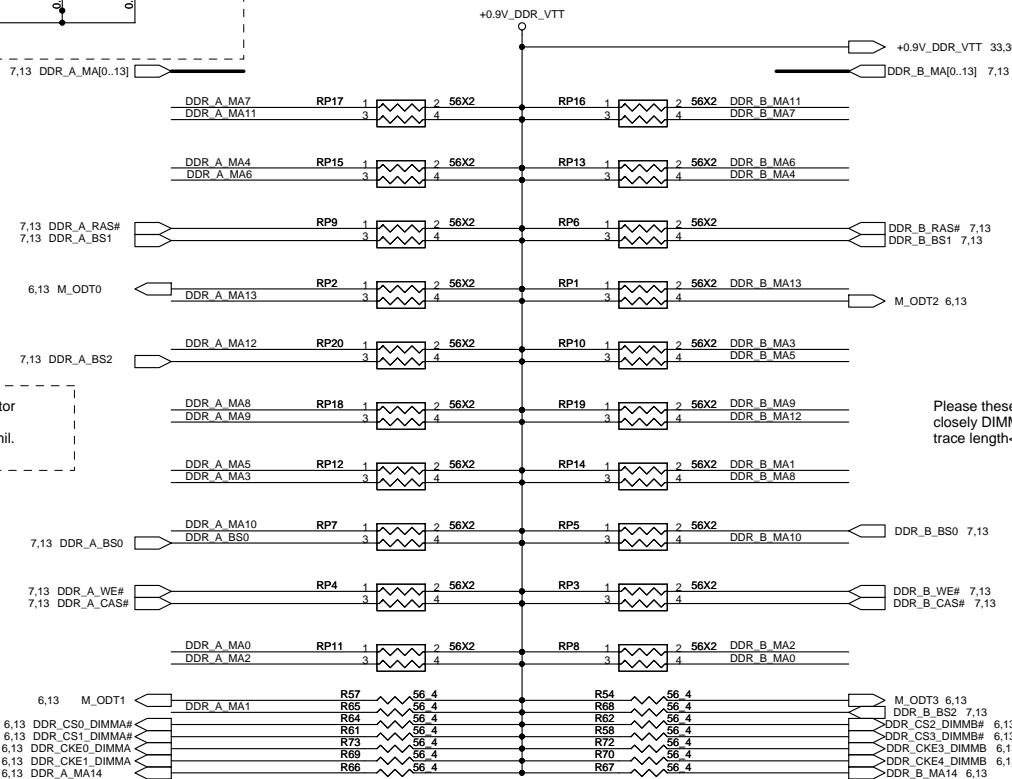
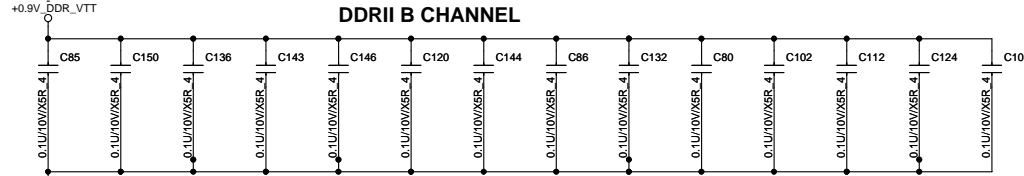


DDRII A CHANNEL

Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

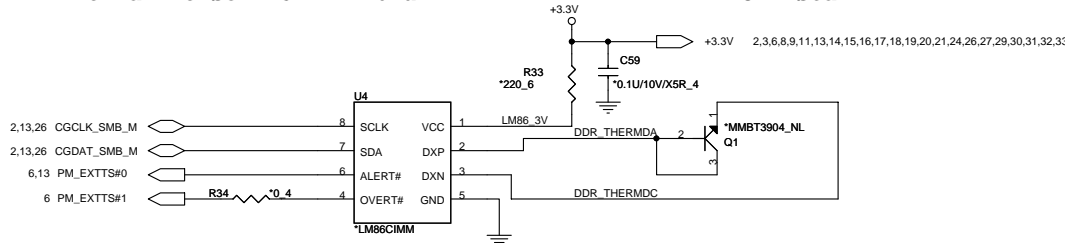


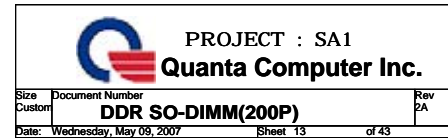
DDRII B CHANNEL

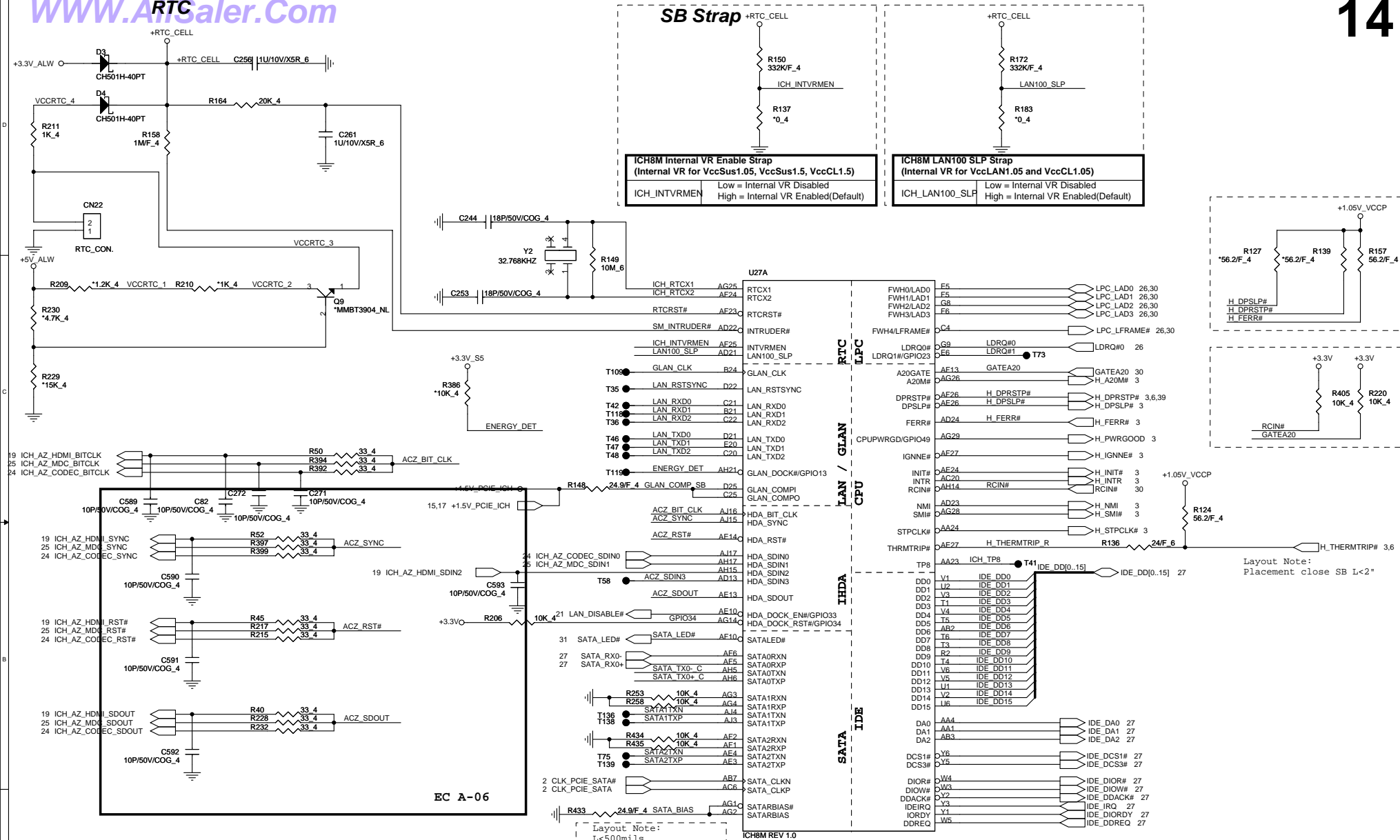


DDR2 Thermal Sensor SO-DIMM 0 & 1

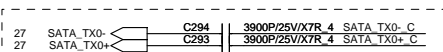
Uninstall







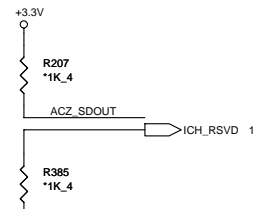
Place all series terms close to ICH8 except for SDIN input lines, which should be close to source. Placement of R430, R434, R199 & R200 should equal distance to the T split trace point as R428, R435, R195 & R204 respective. Basically, keep the same distance from T for all series termination resistors.

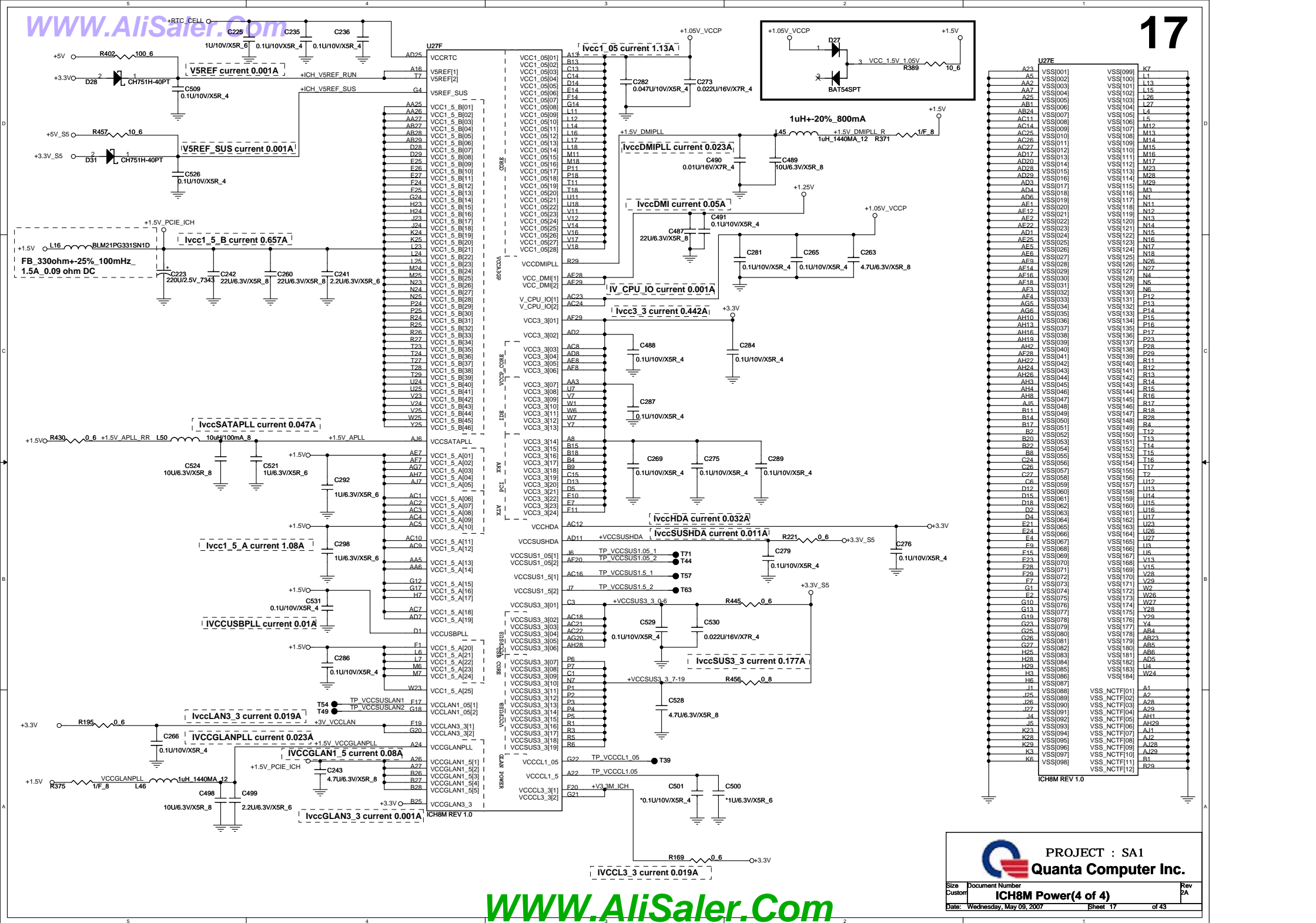


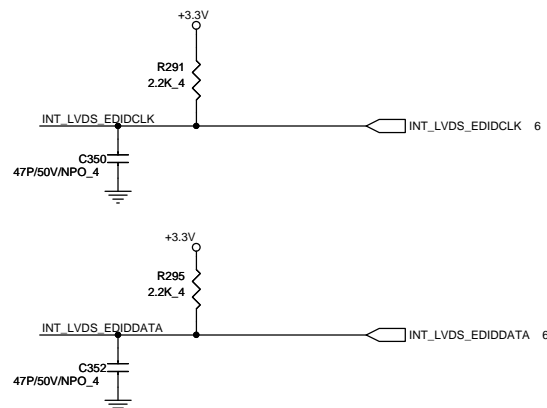
Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-8 M and cap on the "N" signal for same pair.

XOR Chain Entrance Strap

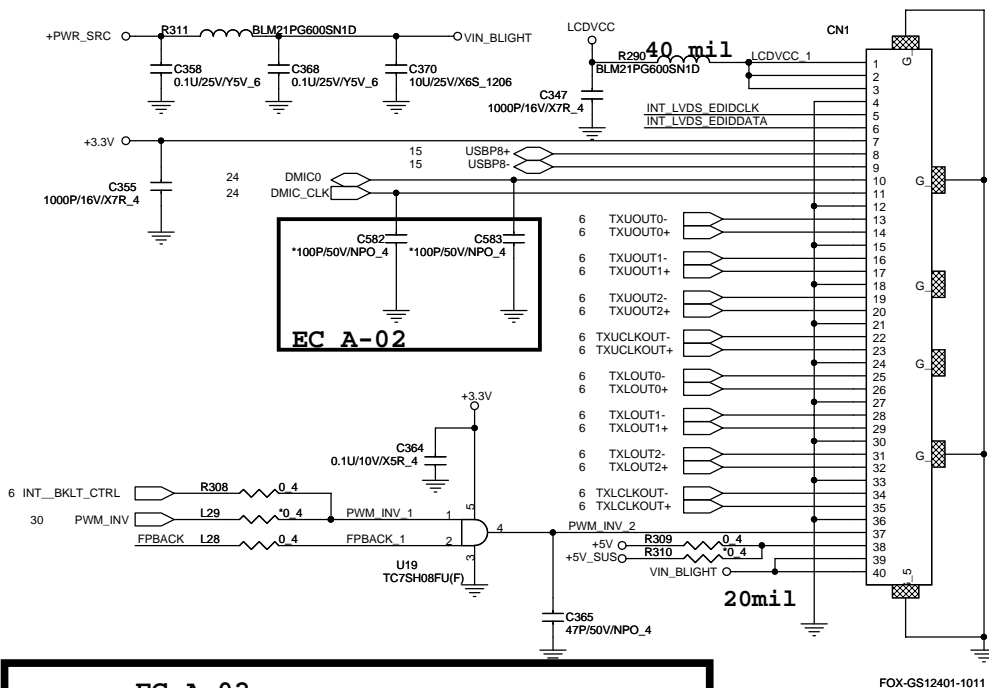
ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIE port config bit 1





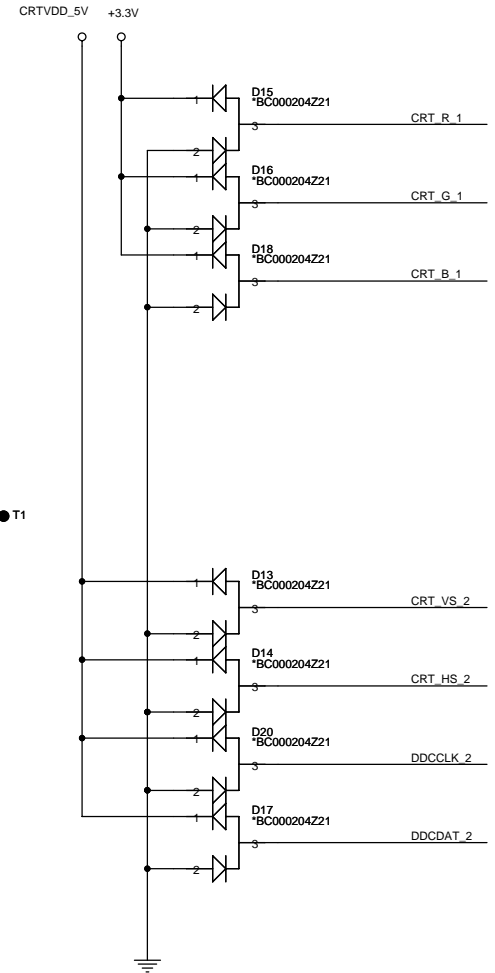
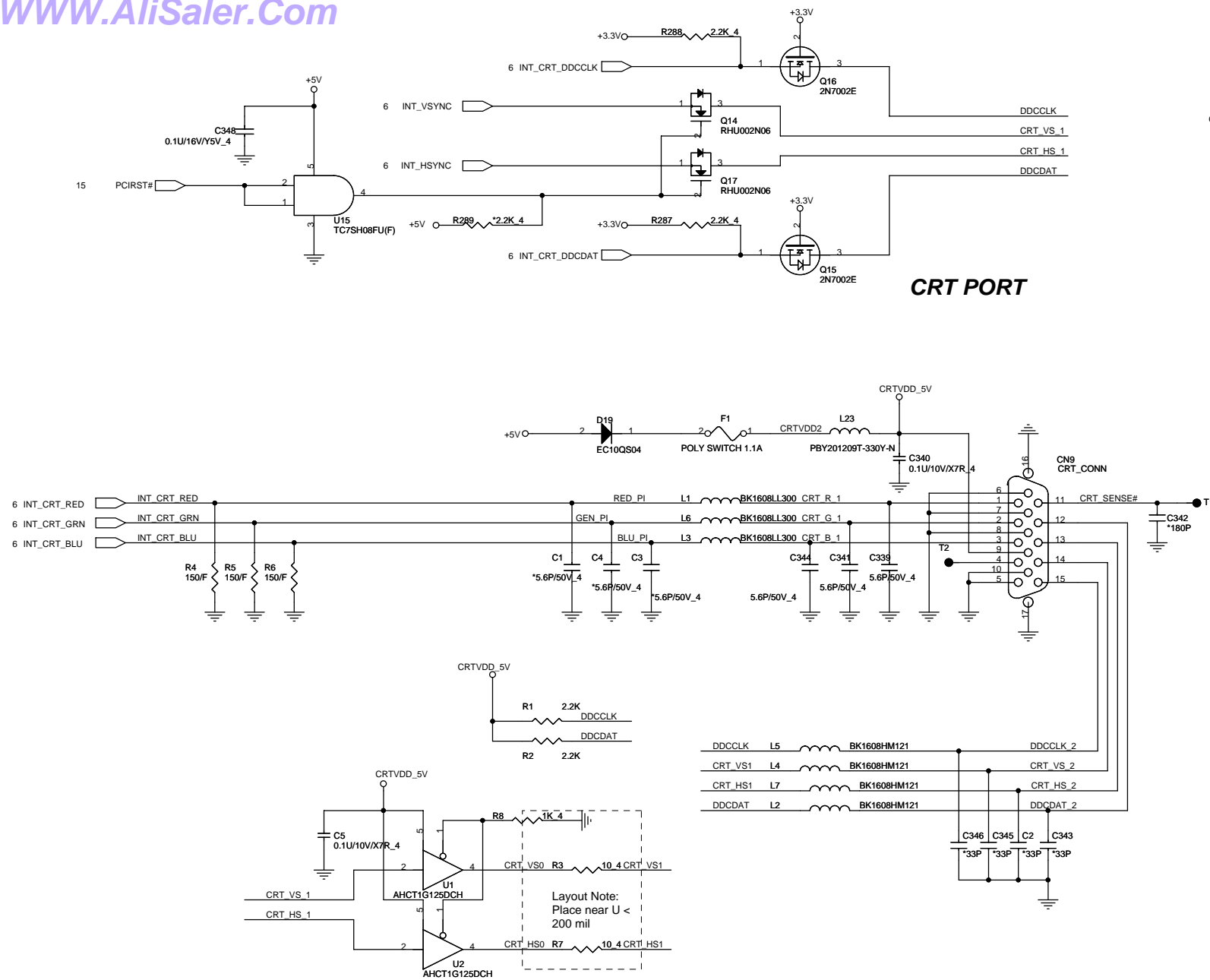


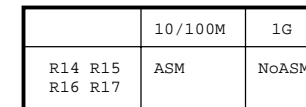
LCD CONNECTOR(Include WEB CAM function)



WWW.AliSaler.Com

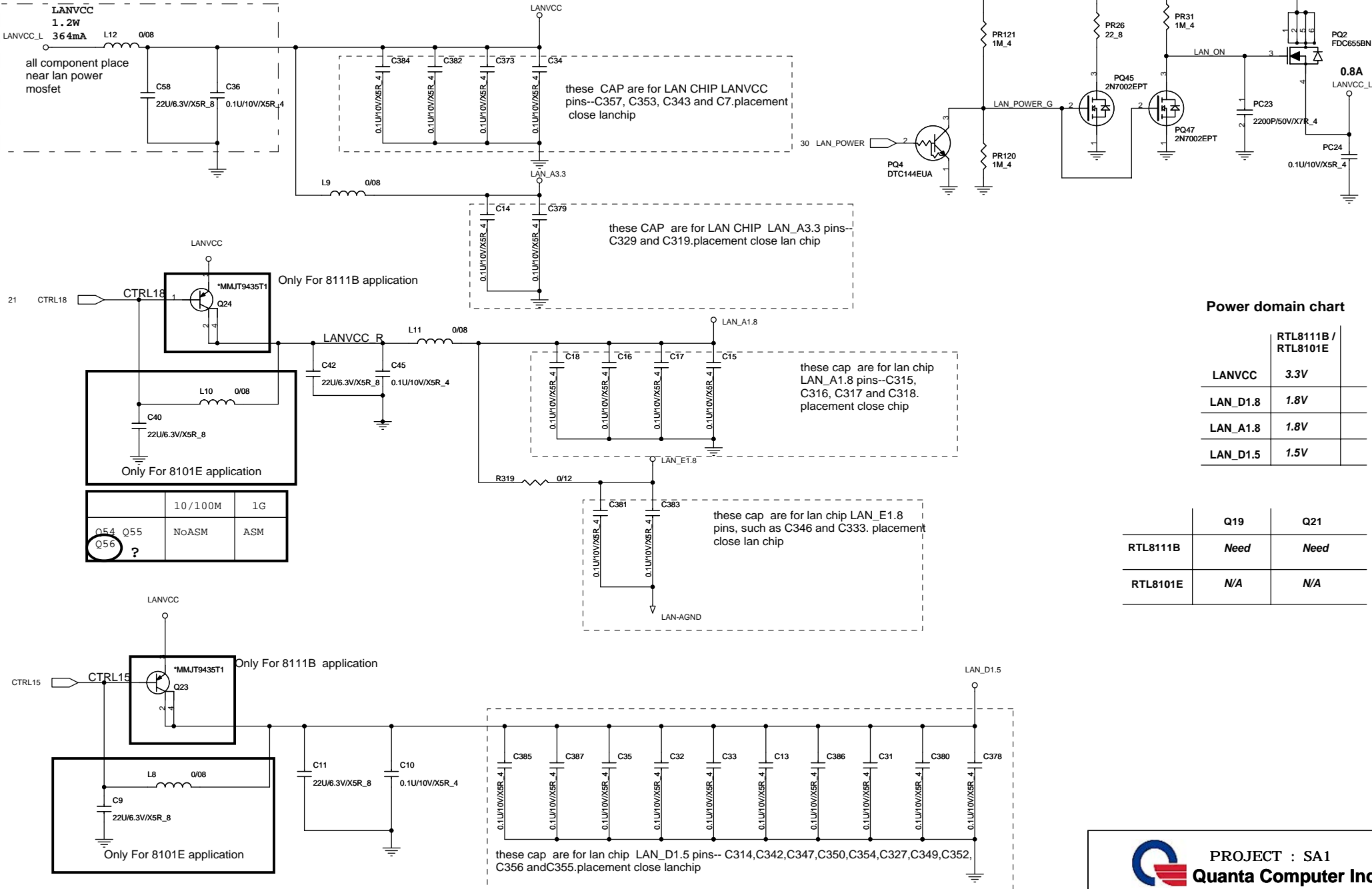
CRT PORT





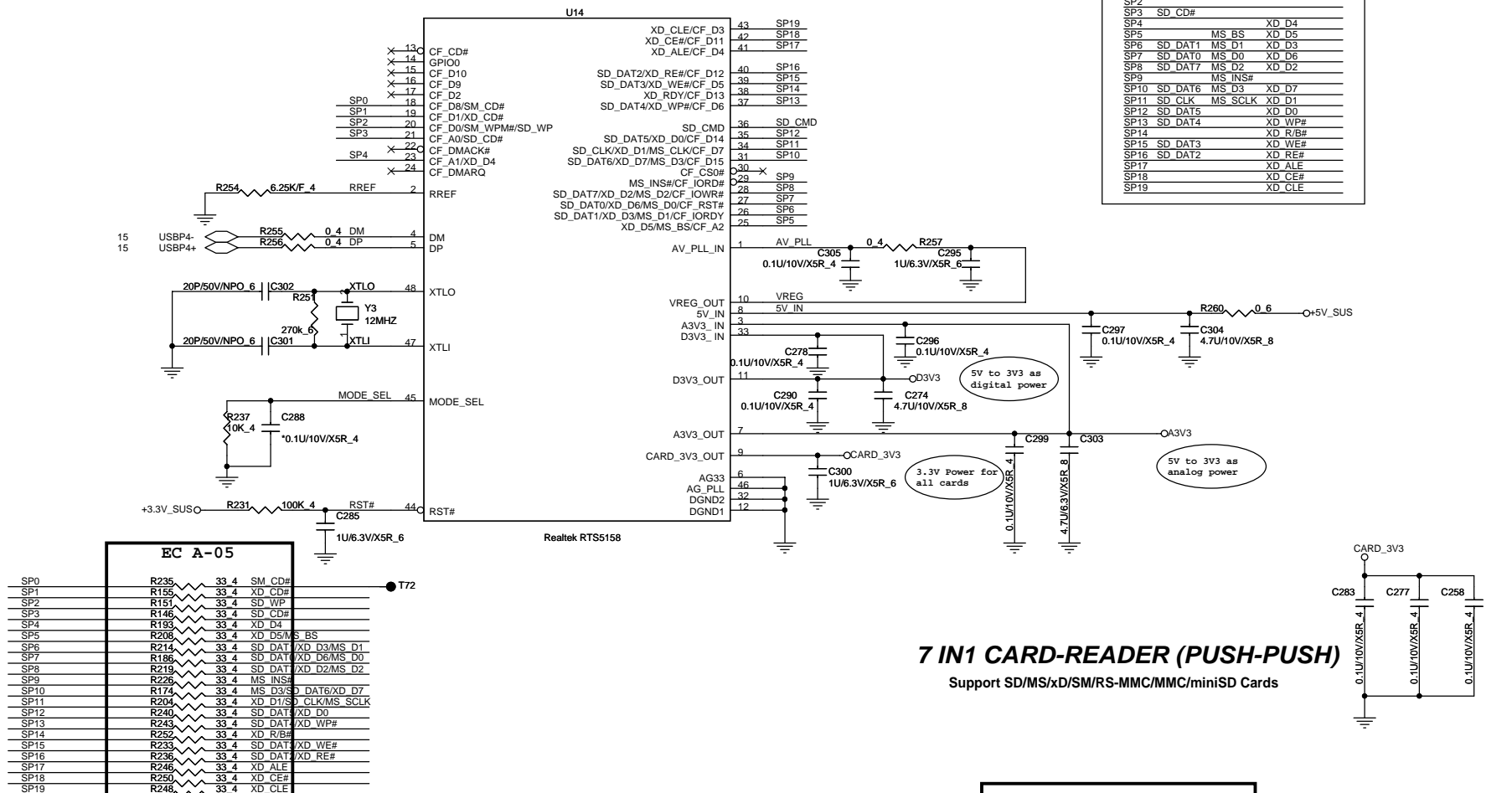
T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)



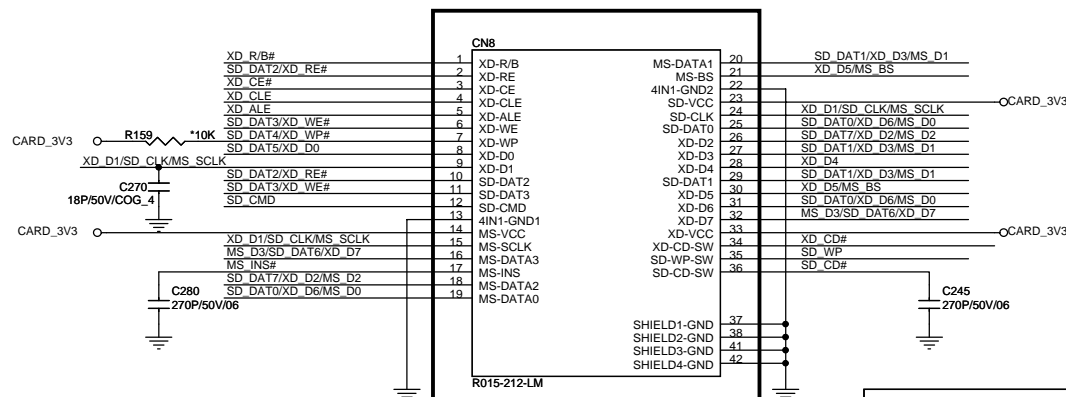
Note:

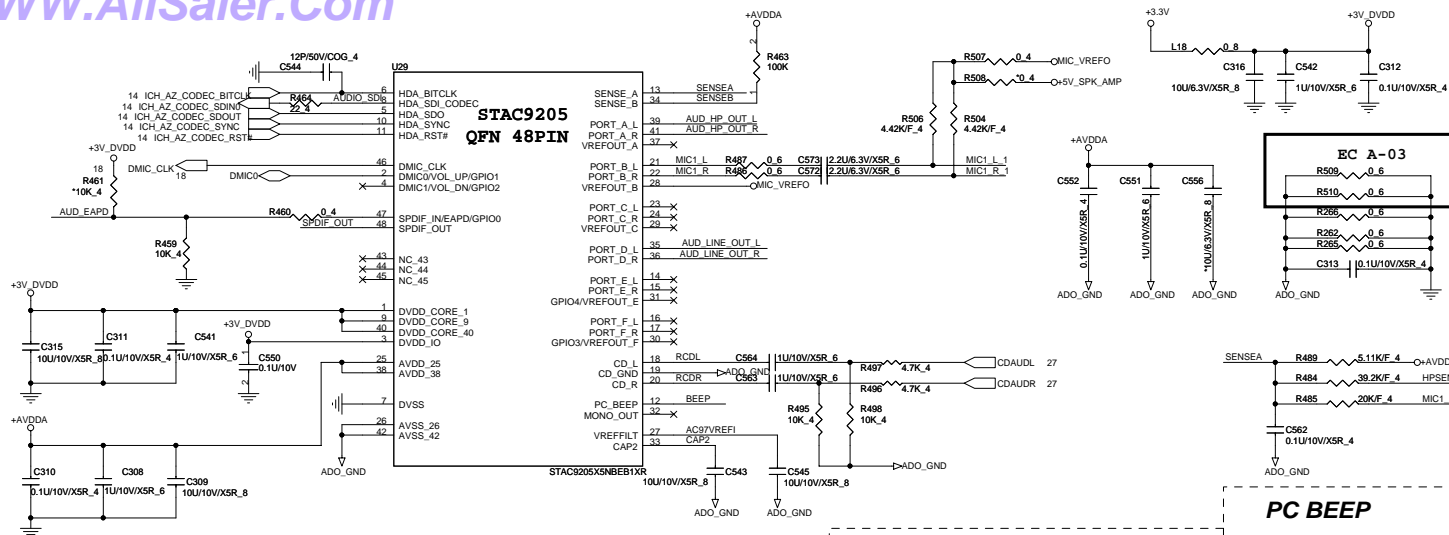
	SD/MMC	MS	XD
SP0	SD WP		XD CD#
SP1	SD WP		XD CD#
SP2			
SP3	SD CD#		
SP4			
SP5		MS BS	XD D5
SP6	SD DAT1	MS D1	XD D3
SP7	SD DAT0	MS D0	XD D6
SP8	SD DAT7	MS D2	XD D2
SP9		MS INS#	
SP10	SD DAT6	MS D3	XD D7
SP11	SD CLK	MS SCLK	XD D1
SP12	SD DAT5		XD D0
SP13	SD DAT4		XD WP#
SP14			XD R/#
SP15	SD DAT3		XD WE#
SP16	SD DAT2		XD RE#
SP17			XD ALE
SP18			XD CE#
SP19			XD CLE



7 IN1 CARD-READER (PUSH-PUSH)

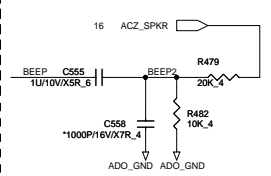
Support SD/MS/xD/SM/RS-MMC/MMC/miniSD Cards





Port A – System headphone Jack (JD : HP_PLG)
 Port B – System Stereo Microphone Jack (JD : MIC1_PLG)
 Port C – System Int. Mono Microphone
 Port D – System Speaker (JD : N/A)

PC BEEP

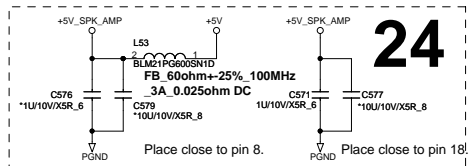


MAX9789A TQFN 32PIN

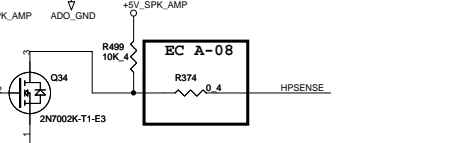
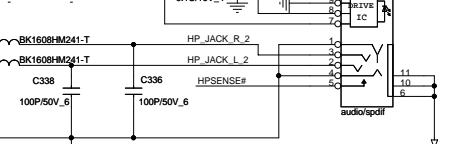
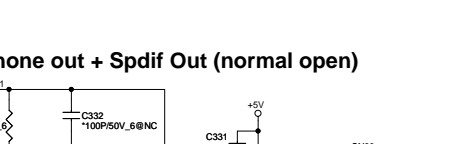
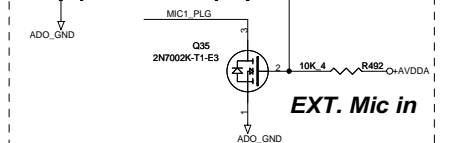
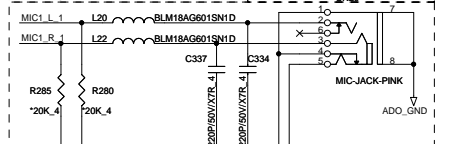
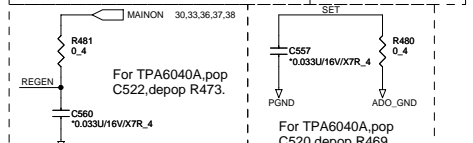
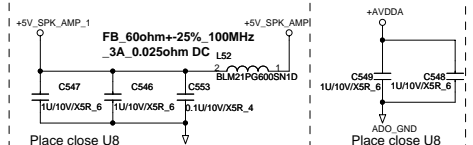
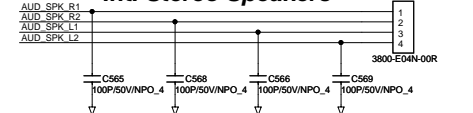
AUDIO AMPLIFIER

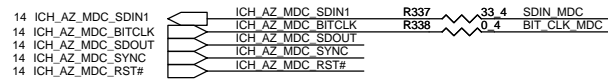
MAX9789A U30

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

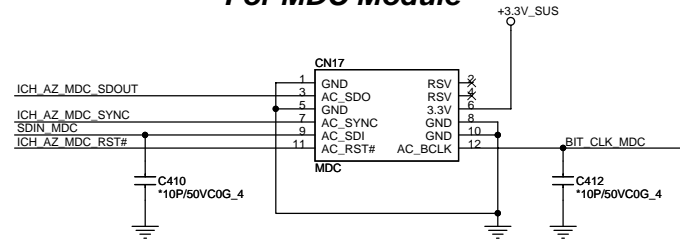


Int. Stereo Speakers

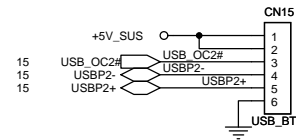


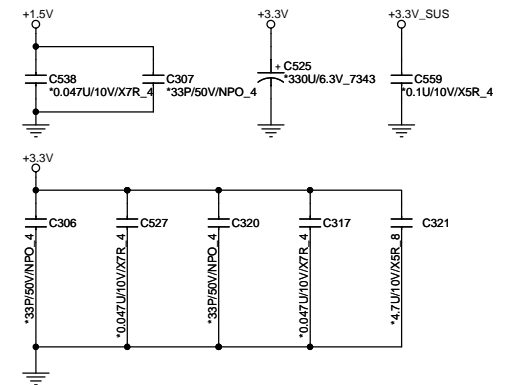
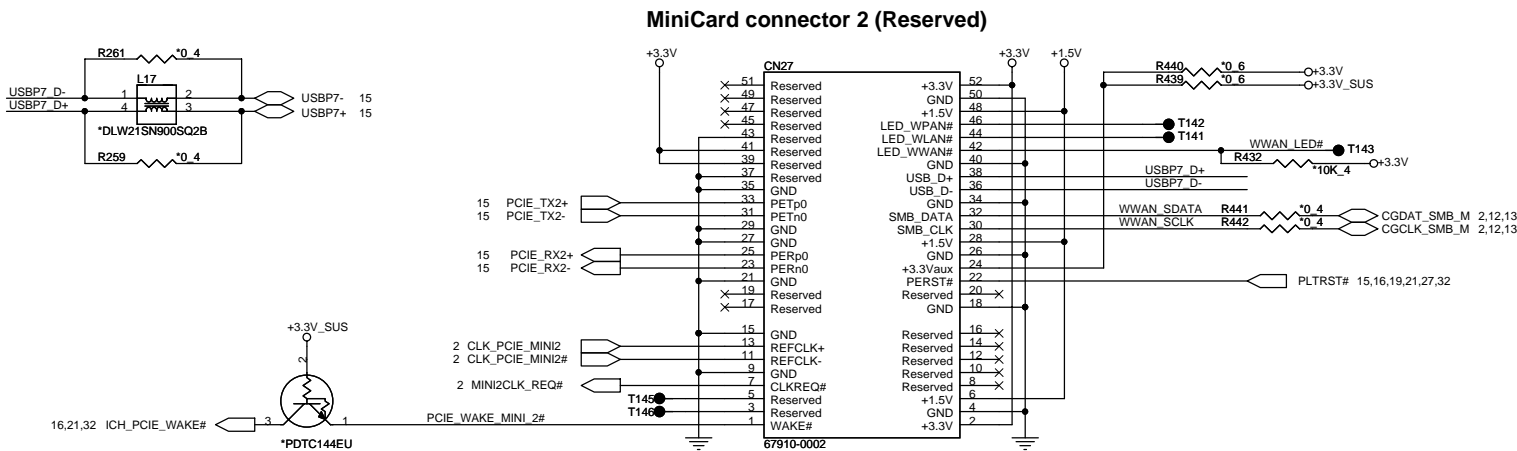
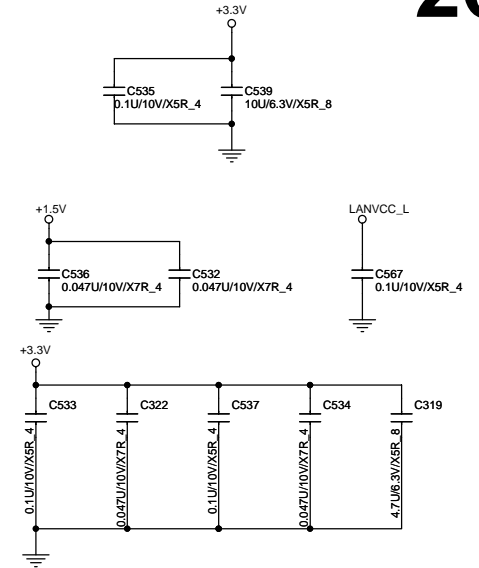
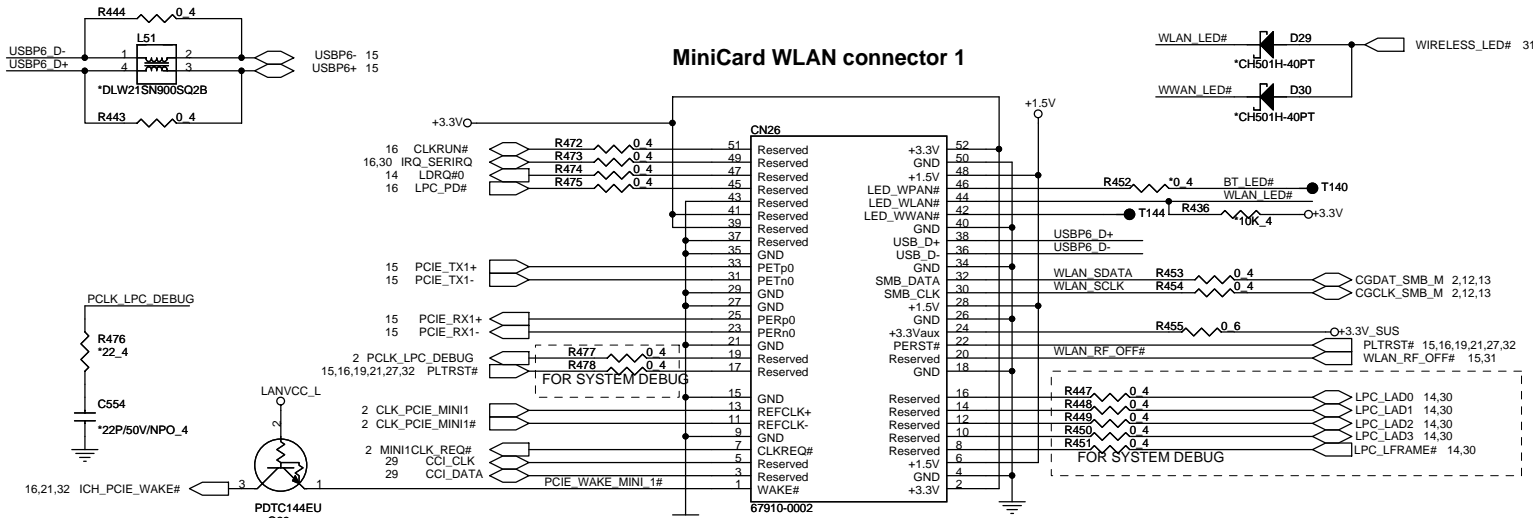


For MDC Module

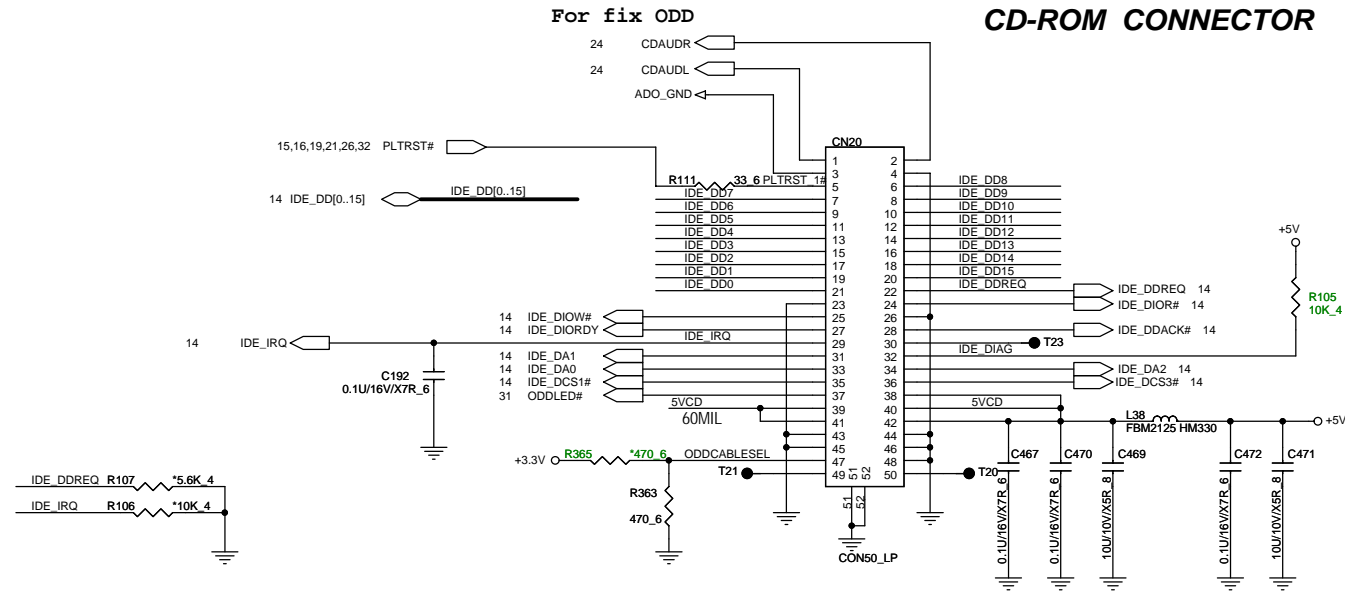


TO RJ11/USB PORT

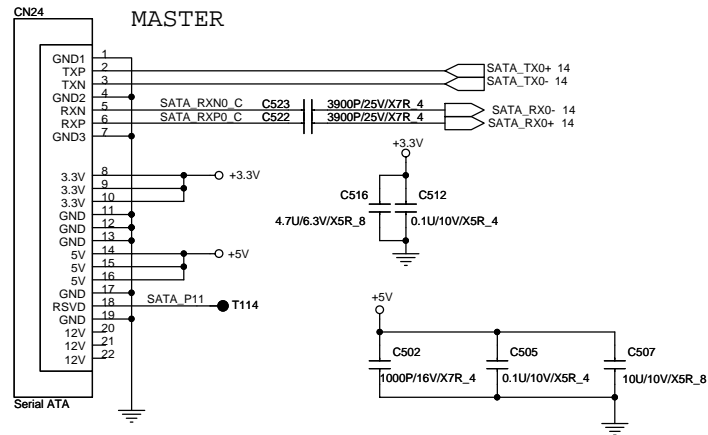


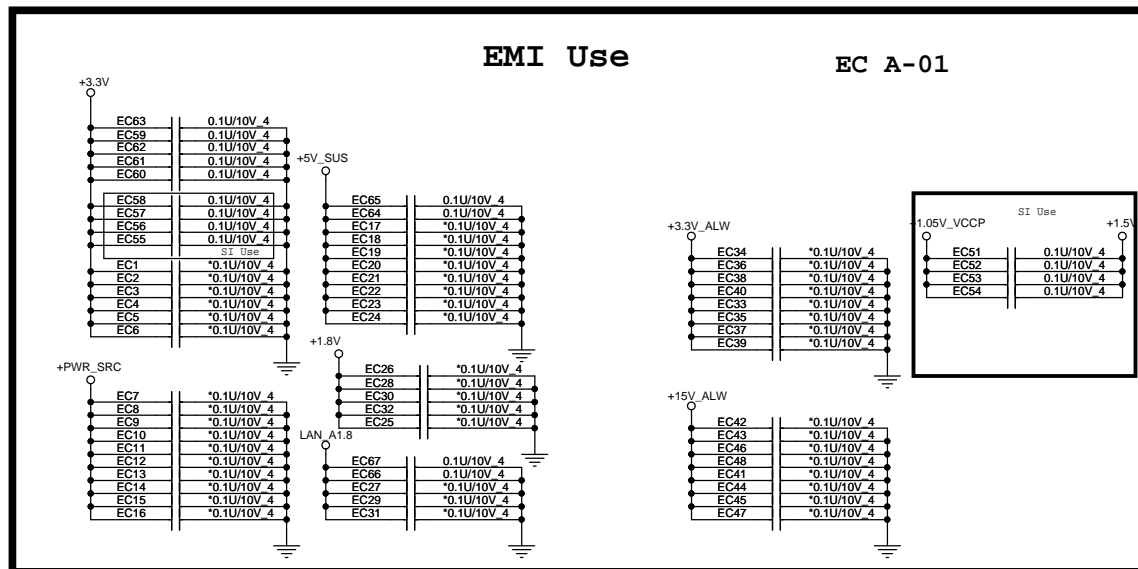
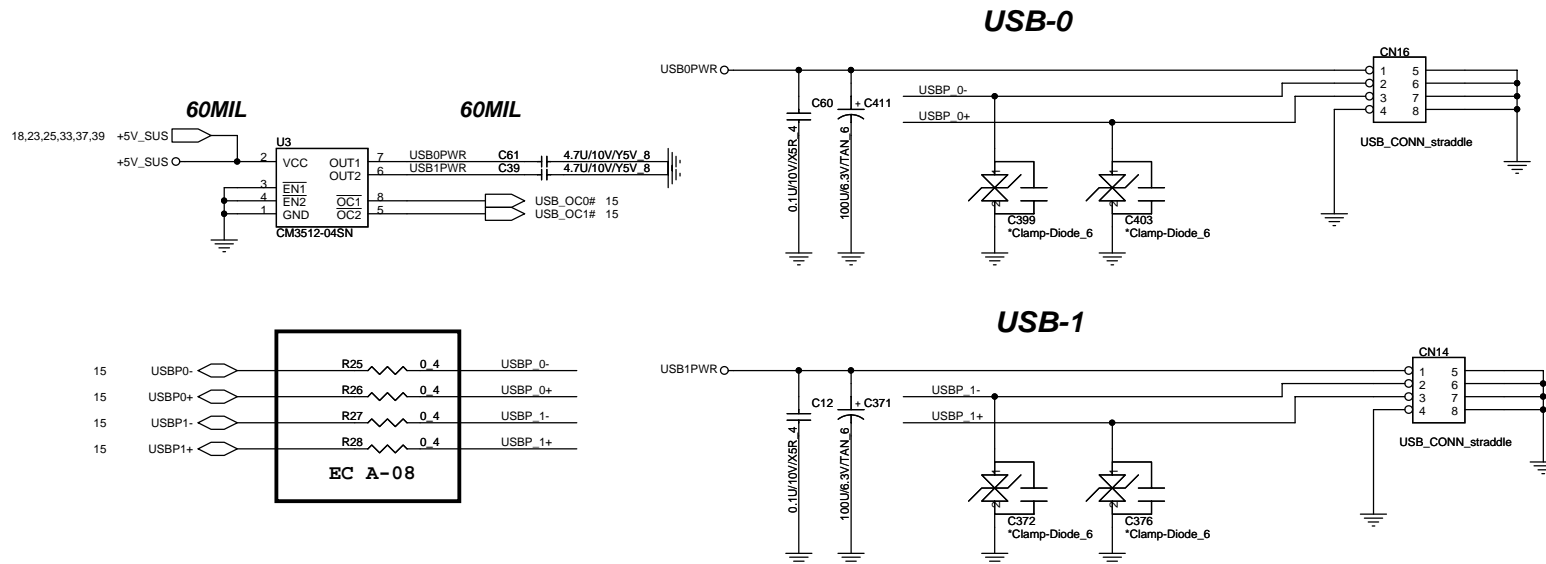


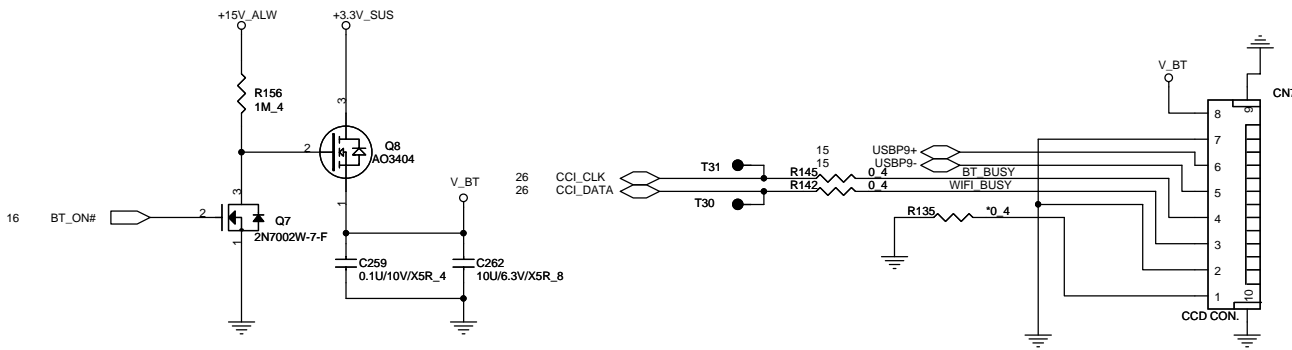
PROJECT : SA1
Quanta Computer Inc.



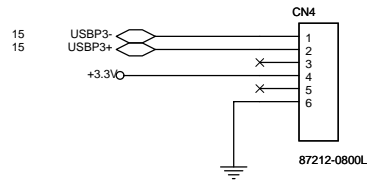
SATA CONNECTOR

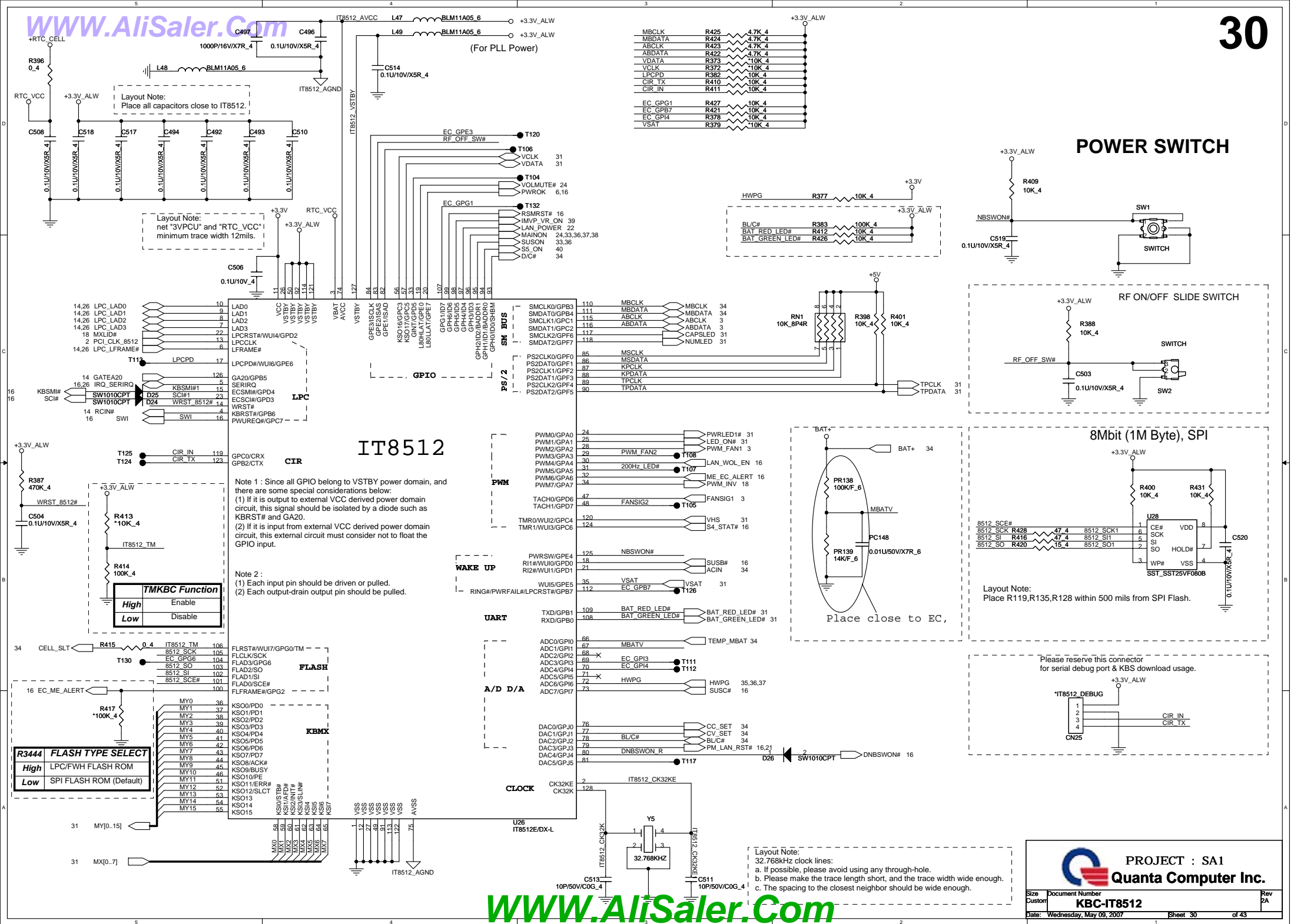




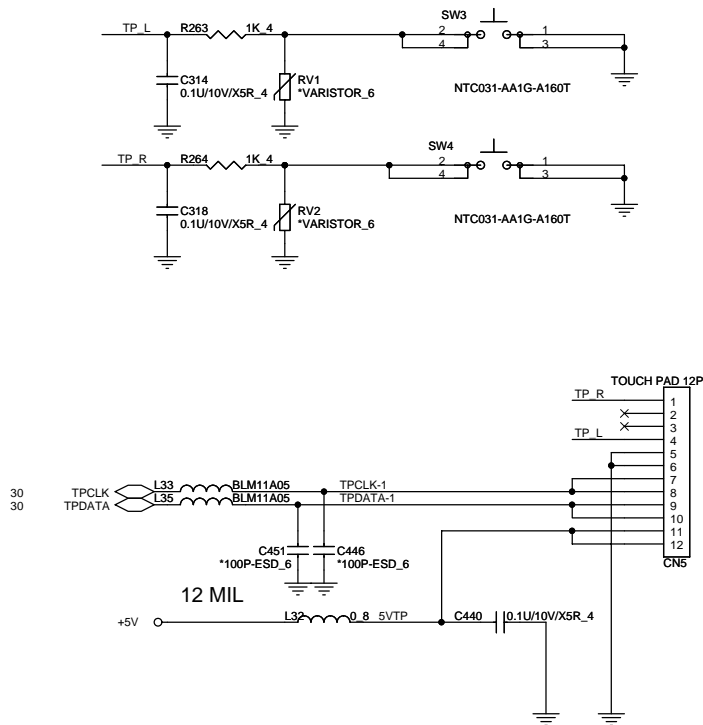


FINGERPRINT CONNECTOR

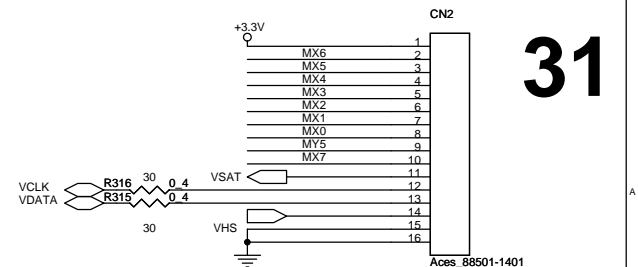
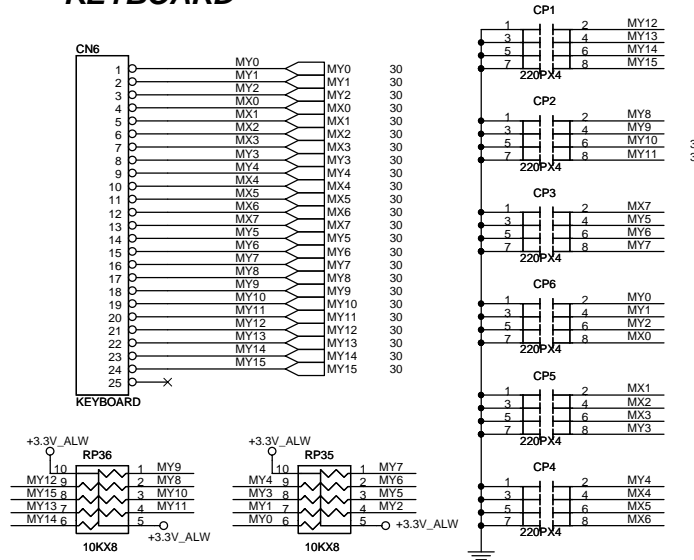




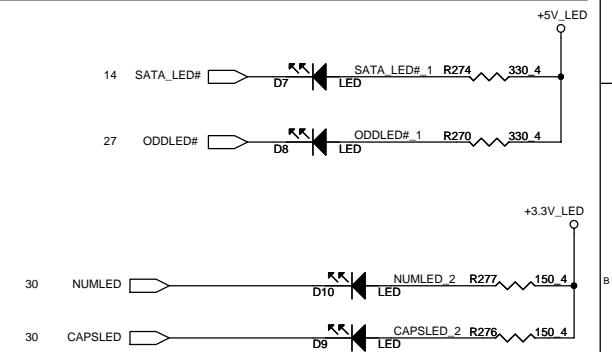
TOUCHPAD SWITCH CONN



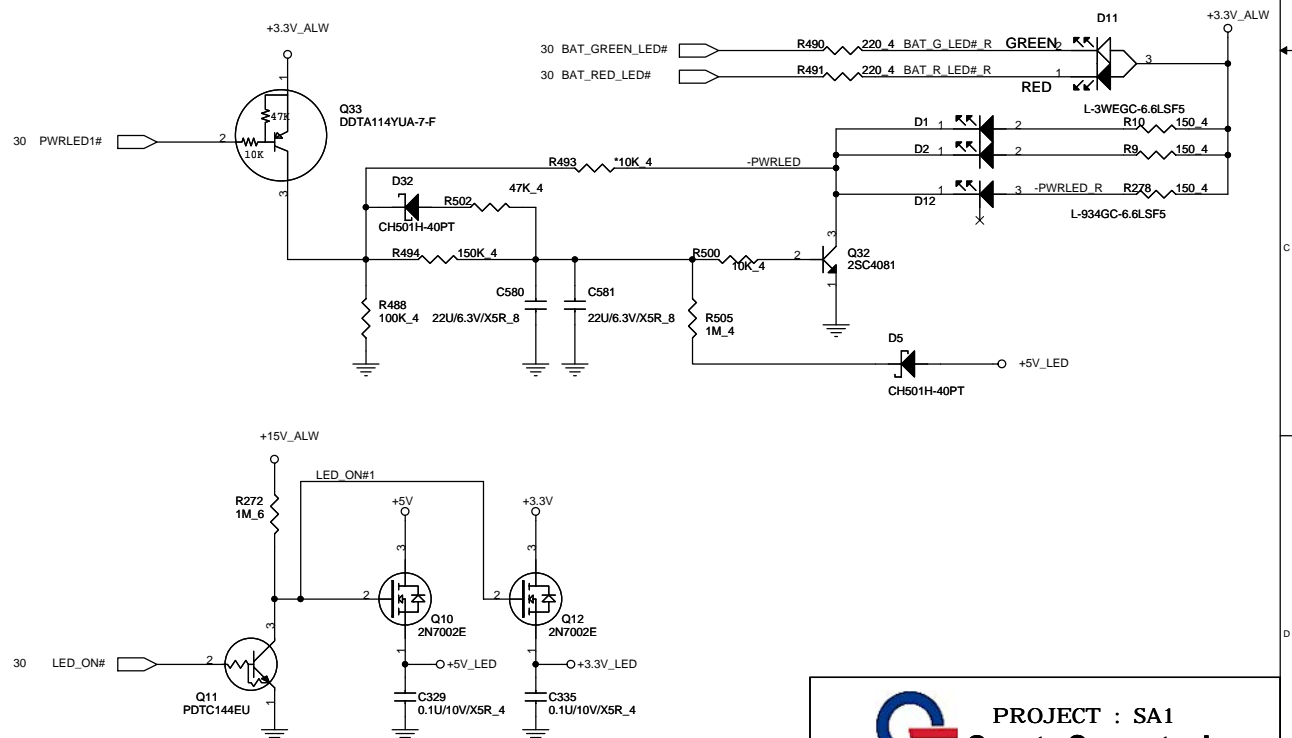
KEYBOARD



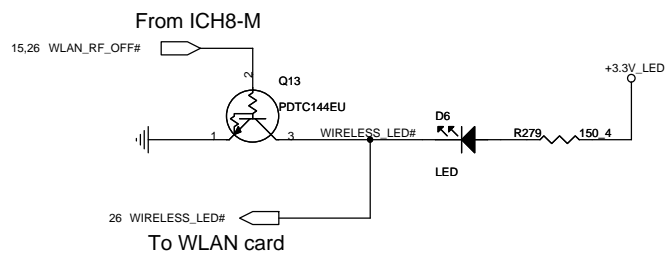
SWITCH/Volume cintral BOARD



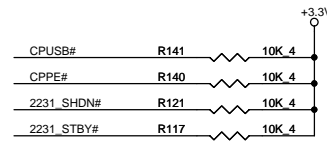
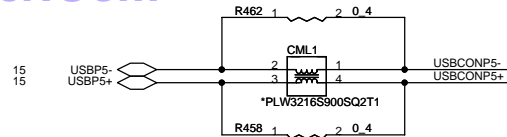
LED INDICATOR



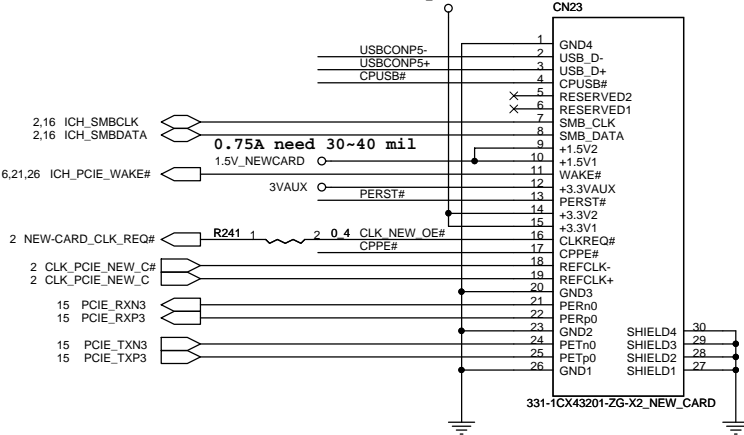
WIRELESS LED



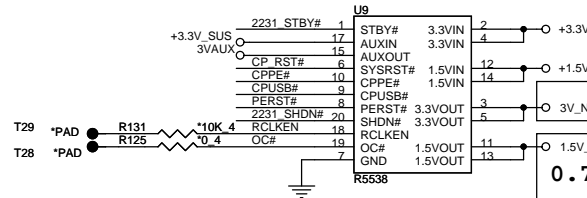
NEWCARD



1.35A need 60 mil

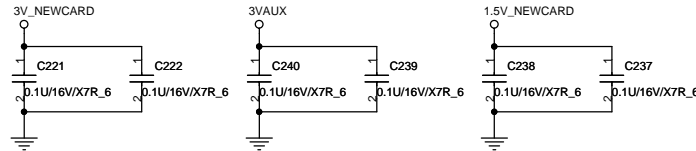
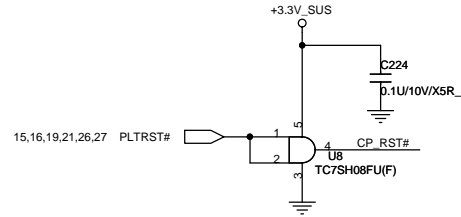


0.75A need 30~40 mil

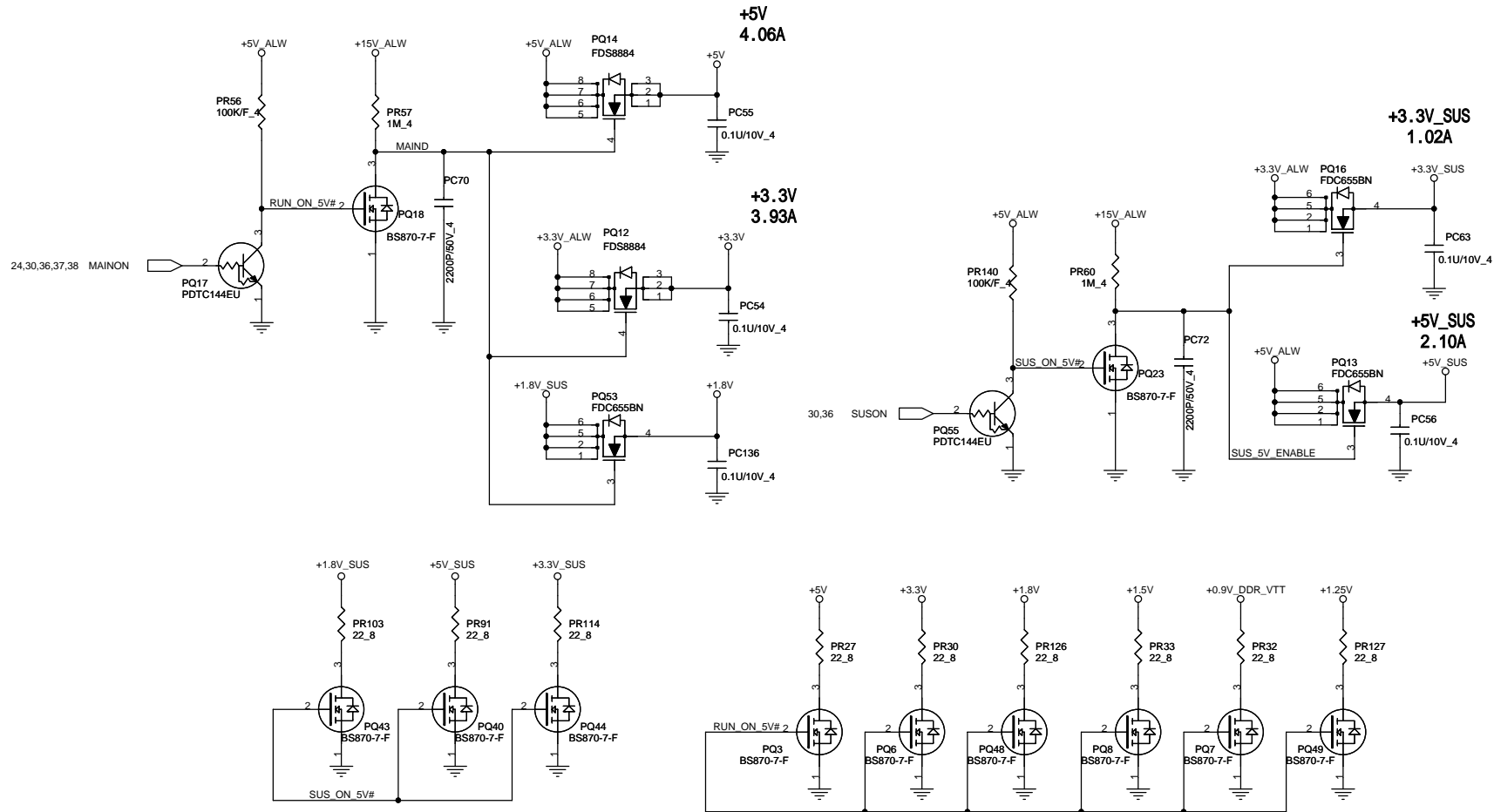


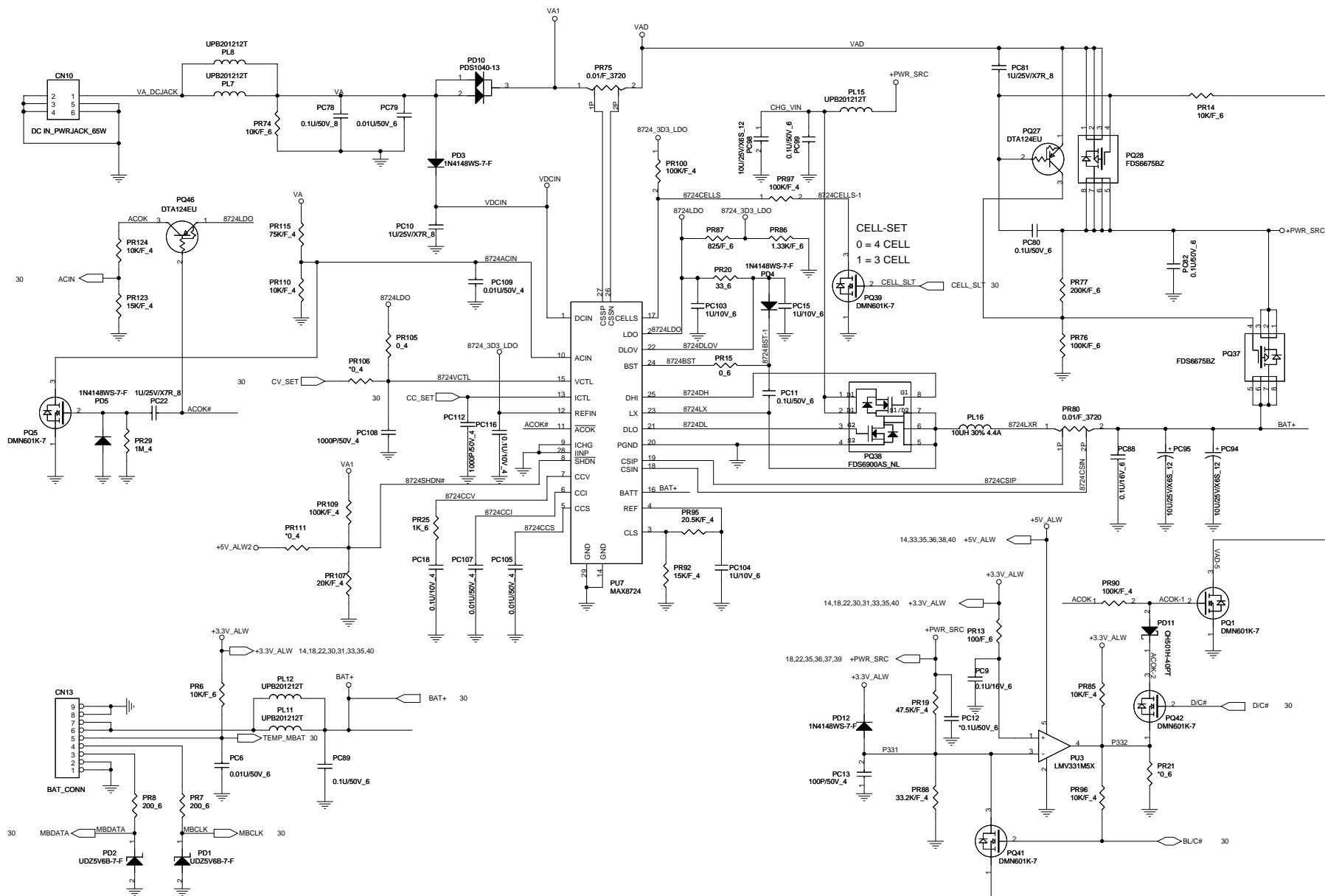
1.35A need 60 mil

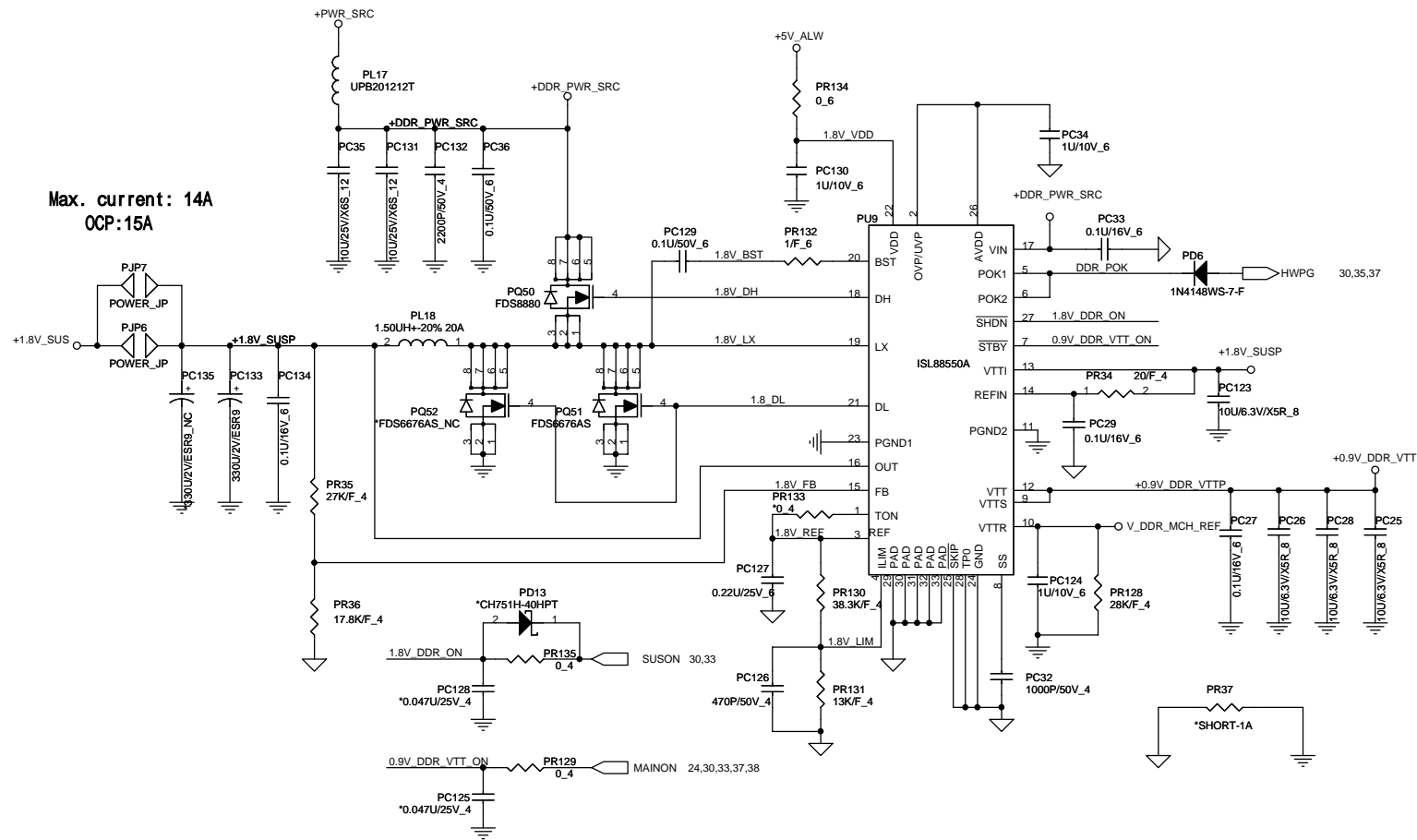
0.75A need 30~40 mil

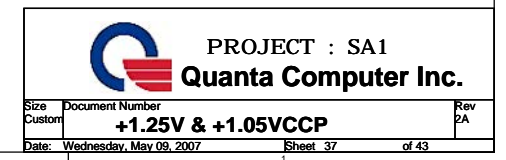


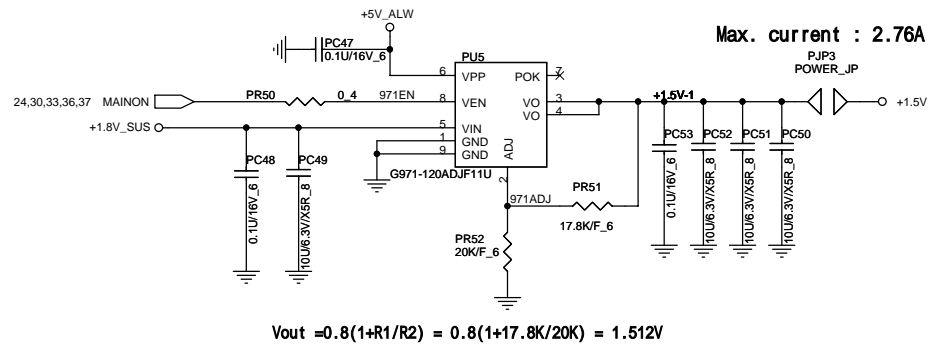
PROJECT : SA1
Quanta Computer Inc.

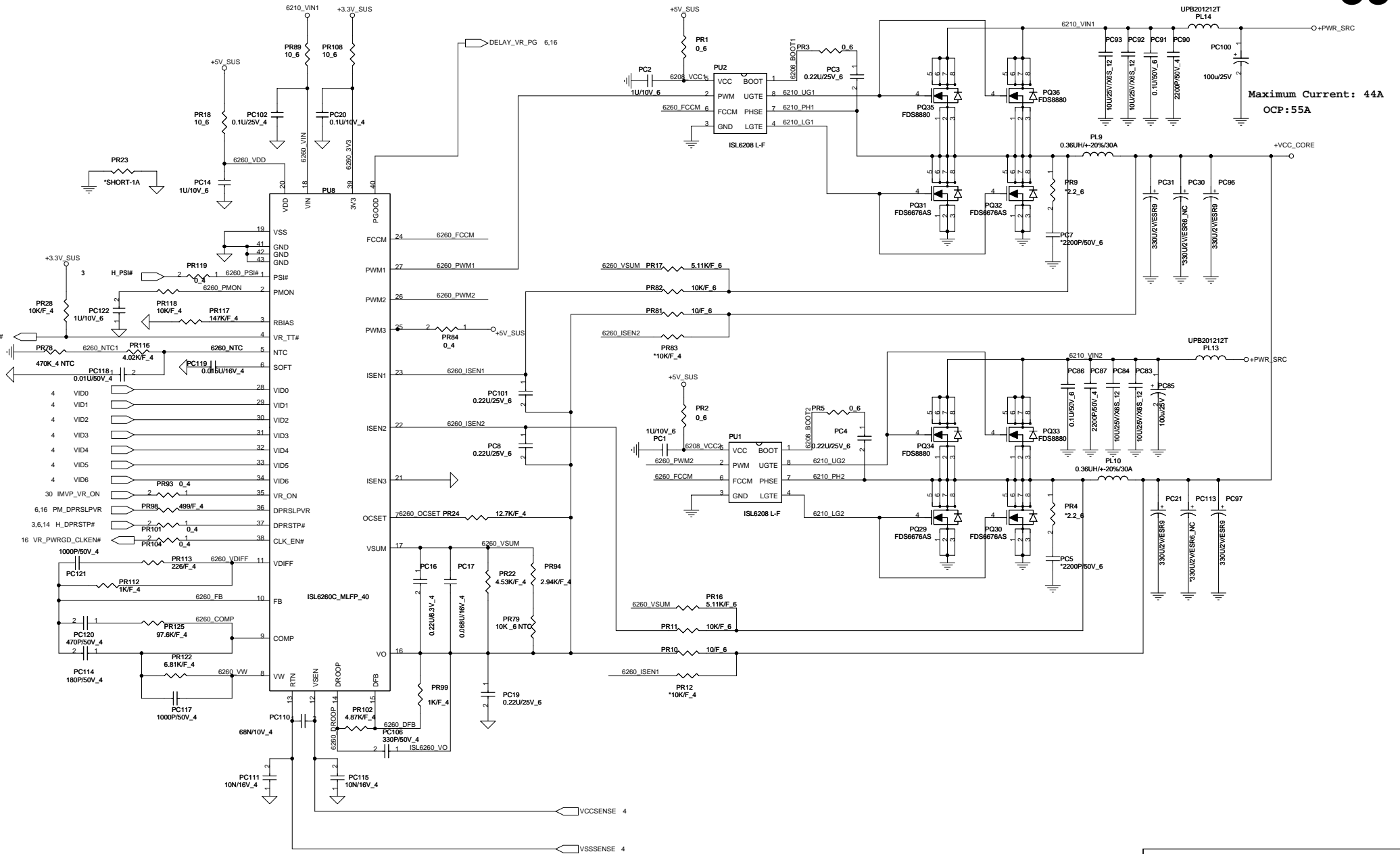








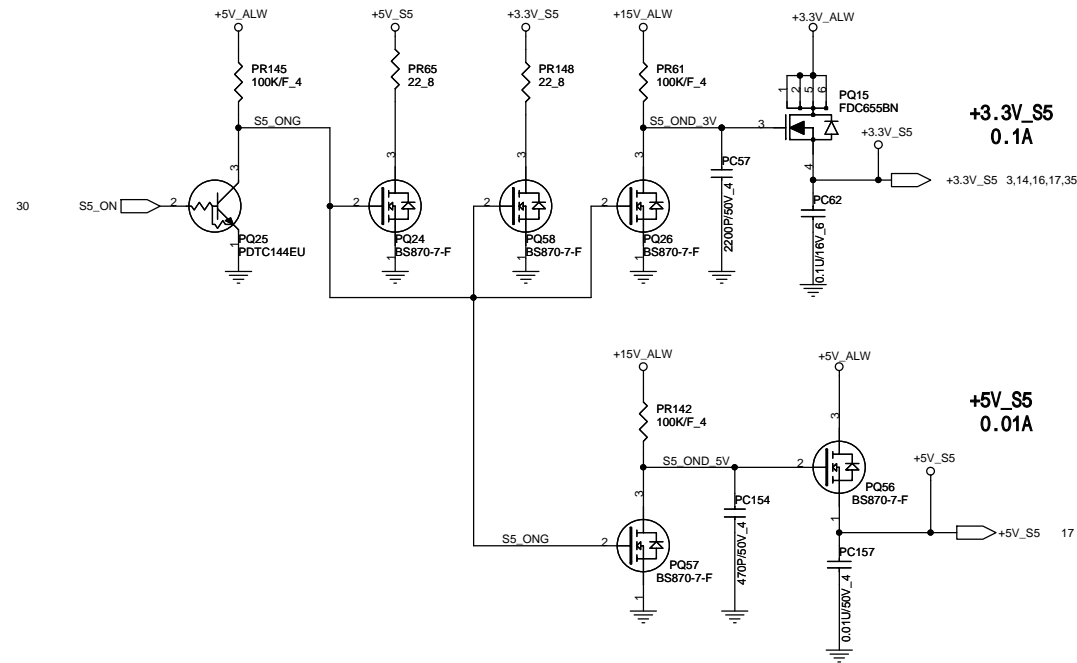


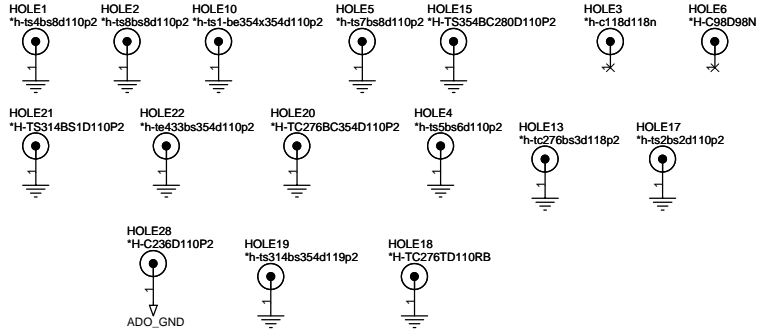
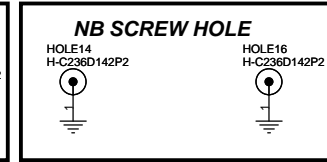
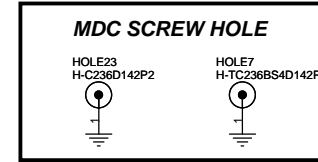
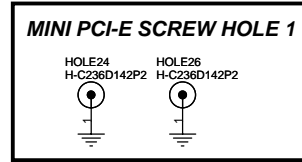
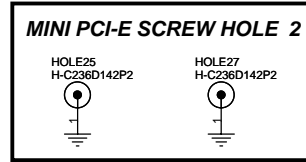
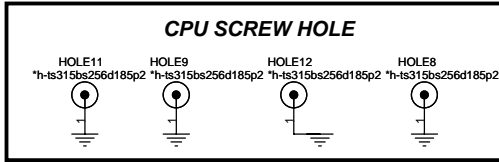


Maximum Current: 44A
OCP:55A



Size: Custom
Document Number: CPU CORE POWER
Date: Wednesday, May 09, 2007
Sheet: 39 of 43
Rev: 2A





EC A-01 /28 Add EMI EC1~EC52 for EMI use
EC A-02 /18 Add EMI EC49, EC50,C582,C583 for EMI use.
EC A-03 /24 Add EMI R509,R510 for EMI use.
EC A-04 /21 CN12 Pin9 and Pin10 connect to GND
EC A-05 /23 Change All SP0~SP19 0 ohm to 33 Ohm
EC A-06 /14 Add EMI request C589~C593
EC A-07 /6 Add EMI request C594~C595
EC A-08 /24 Add R374 0 Ohm for Audio SPDIF Detec.
EC A-09 /28 Remove EB2 for EMI.
EC A-10 /19 Add R?~R? for Fix SDVO issue